

# **NSING MCU Download Tool User Manual**

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## **1 The introduction**

### **1.1 Writing purpose**

This helps r&d personnel and production testers understand how to download tools

### **1.2 The reader object**

R&d personnel and production testing personnel.

### **1.3 The term is commonly used**

<b>The term</b>	<b>Instructions</b>

### **1.4 The resources**

## 2 Overview

This document is used to explain and standardize the operation and process of the chip download tool, and is suitable for managers and production operators.

NSING MCU Download Tool is a program download tool for N32G(WB)45x\_FR, N32G(L)43x, N32L40x, N32G032, N32G030, N32G031, N32G430, N32A455, N32G401, N32G003, N32G05x, N32H47x, N32H48x, N32H78x, N32H76x, N32G033 series chips of National Technology. The tool provides chip program download and related configuration functions. UART, USB (DFU), SWD (CMSIS-DAP) communication mode download, support offline downloader project configuration, etc.

## 3 Systematic review

### 3.1 System Function Introduction

The main interface of the download tool is shown in the following figure, which includes selecting devices, downloading operations, files, common operations, displaying test results, and help.

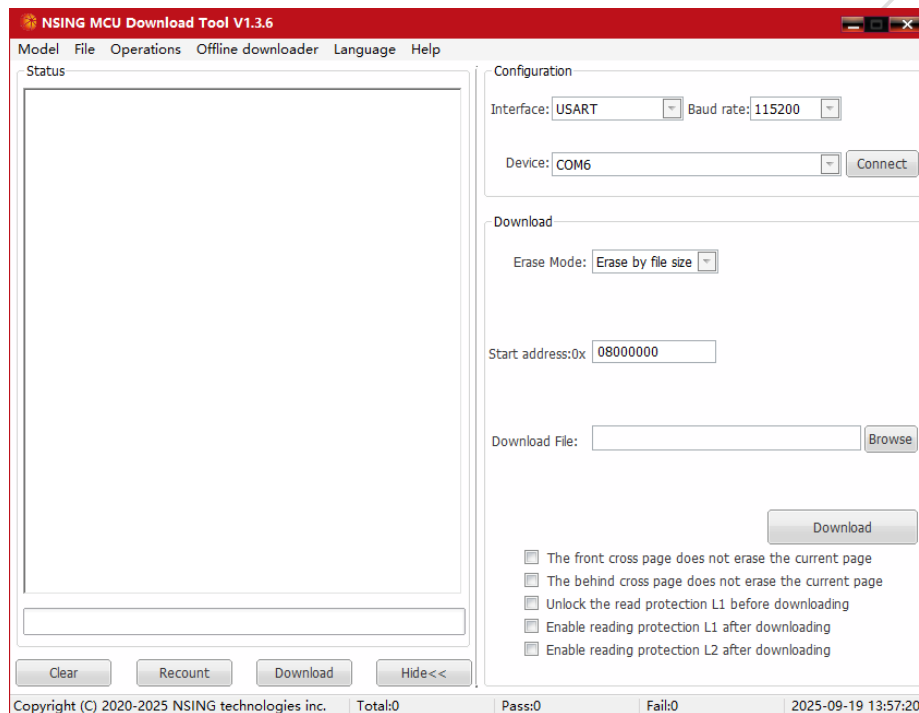


Figure 3-1 Main interface of download tool

### 3.2 System performance

The system resource footprint is very small when the program is running, with both CPU usage and memory footprint less than 1% when the program is running at full speed.

## 4 Runtime environment

### 4.1 Hardware Requirements

The following list shows the minimum configuration of the PC hardware required by this software:

1. CPU Celeron 400MHz or Pentium 133MHz or above
2. The minimum memory size is 128 MB (256MB or more is recommended).
3. The hard disk has more than 100MB free space
4. Monitor with a resolution of 800\*600 or above, 1024x768 or higher is recommended

## **4.2 Software requirements**

The program can run on the 32-bit operating system Windows XP, and supports both 32-bit and 64-bit Windows7 and Windows 10.



## 5 Installation and initialization

This system does not need to install, directly click to run. After the device is correctly connected, the interface after the program is started is as shown in the figure:

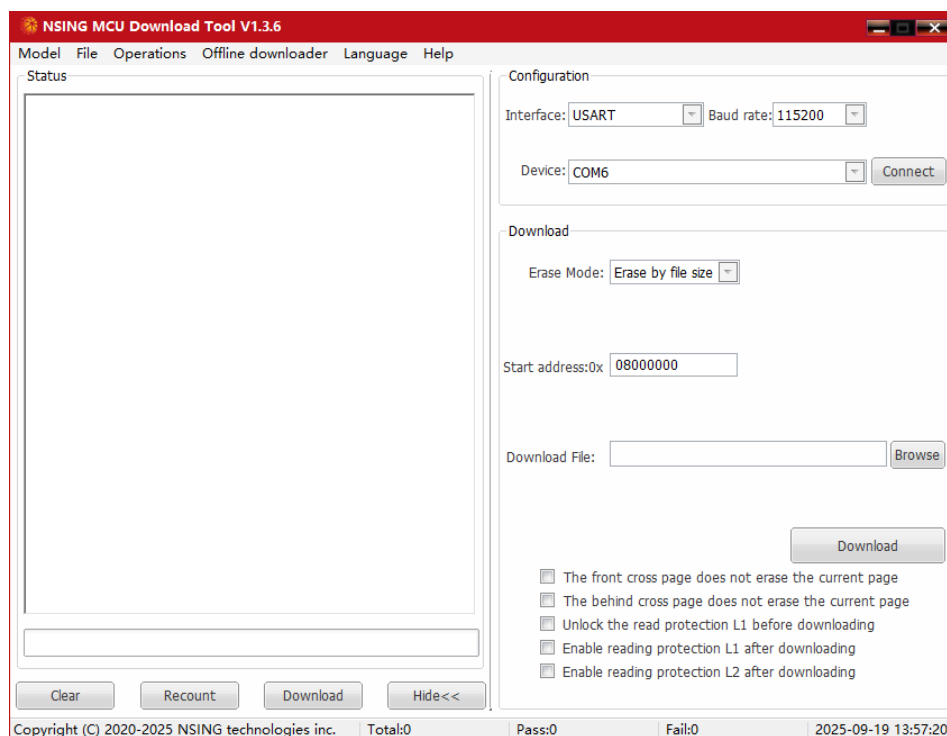


Figure 5-1 Program startup interface

After connecting to the device through the USB port through the UART communication port, you can view the serial port number in the device manager port. If no device is identified, you may need to install a serial port driver. Multiple serial ports are listed when you open the download tool. Select the corresponding device according to the serial port number of the device in device Manager. Correctly identify the equipment as shown in the picture below:

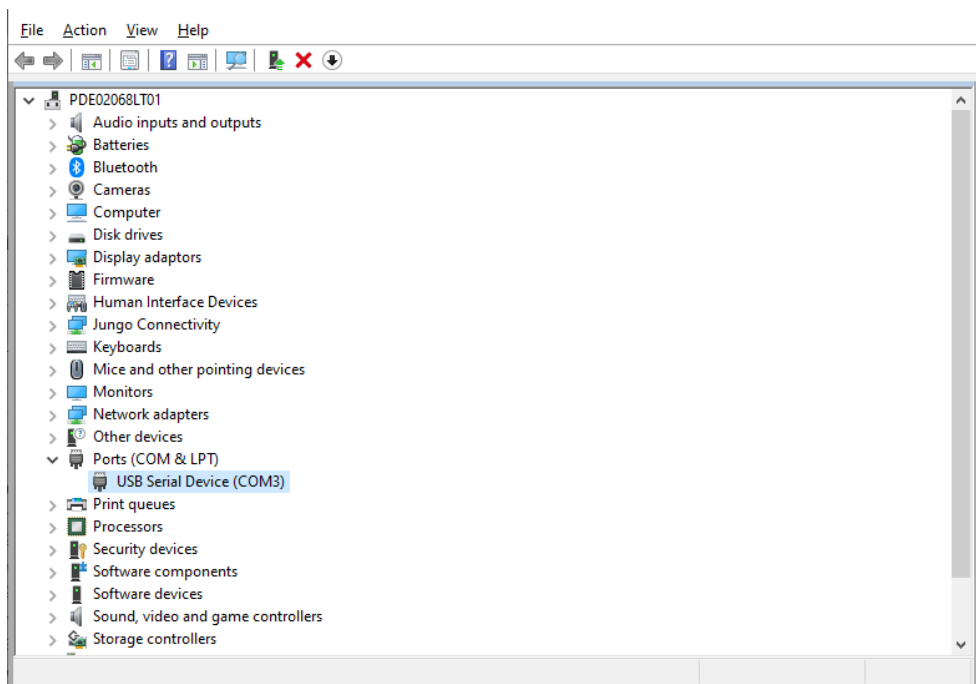


Figure 5-2 Confirm device through Device Manager (UART interface)

Connect to the device through the USB port through the DFU. You need to install the driver for initial connection. Check whether the device is detected by viewing the device manager. Correctly identify the equipment as shown in the picture below:

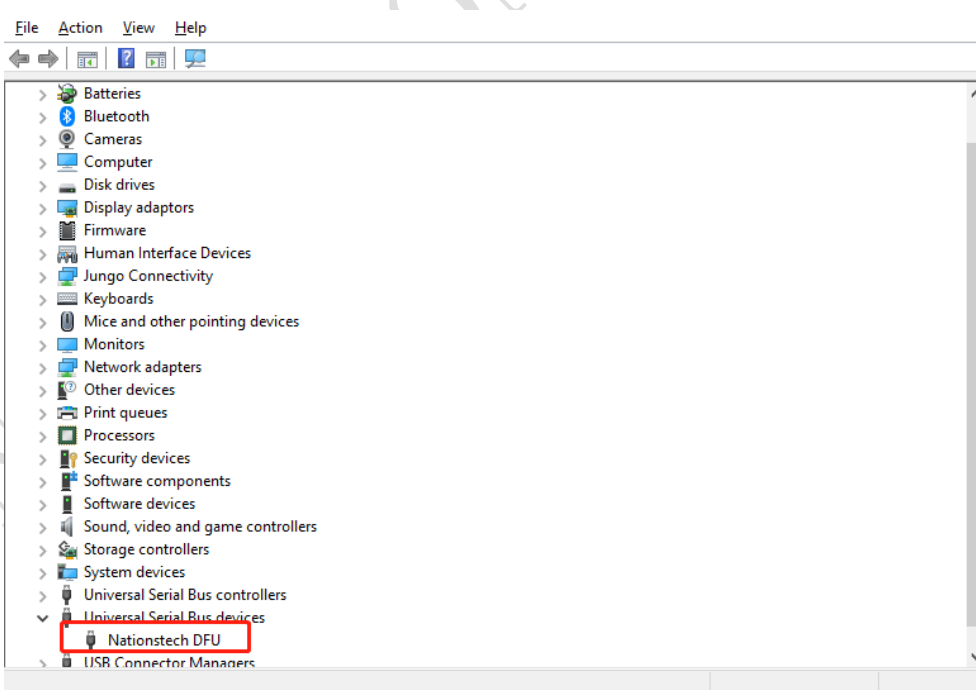


Figure 5-3 Confirming the device through device Manager (USB(DFU) interface)

## **6 Select device Interface**

### **6.1 USART interfaces**

Serial port download interface. When the target chip enters Boot, you can use the serial port to configure the target chip partition, modify the key, operation option bytes, program download and other functions.

### **6.2 USB (DFU) port**

USB download interface: When the target chip enters the BOOT state, USB can be used to connect the target chip, and the target chip partition configuration, modify key, operation option bytes, program download and other functions.

Note: THE USB DFU interface is only available for chips with USB peripherals.

### **6.3 SWD (J-link) interface**

Jlink connection interface. You can use this interface to connect to JLink and use the JLink downloader to perform option byte manipulation on the target chip.

Note: This interface can temporarily only operate on option bytes to enable read protection and remove read protection.

### **6.4 NS-Link-Pro Interface**

This interface is used to connect the NS-Link-Pro offline downloader for communication between the offline downloader and the PC.

### **6.5 SWD (CMSIS DAP) Interface**

This interface can be used to obtain chip information, erase operation option bytes, operation read-write protection, program download, read flash and other functions for the target chip.

## **7 Online download**

For online program download, the target chip must enter Boot state and download in USART

(serial port) or USB (DFU) mode.

## 7.1 USART program download

### 7.1.1 Select equipment

Take the USART interface as an example, connect the development board and PC correctly through the USB-to-serial cable, pull the target chip BOOT0 pin high, reset or re-power the target chip, and make the target chip enter the BOOT state. Open the tool and check whether the current device can be enumerated (take N32G033 series chips as an example), as shown in the figure:

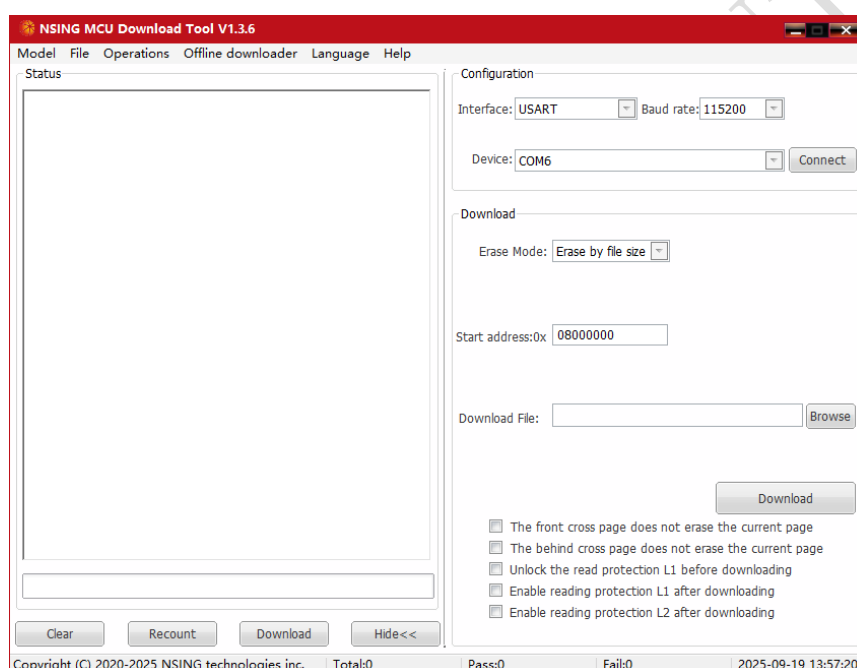


Figure 7-1 Selecting a device

### 7.1.2 Connected devices

Users can select baud rate as required (the default value is 9600), such as 115200, and then click "Connect Device" button. After the device is successfully connected, "Connect Device" turns to "Disconnect Device" and the status displays the chip model, BOOT version number, FLASH capacity and other information of the current chip, as shown in the following figure:

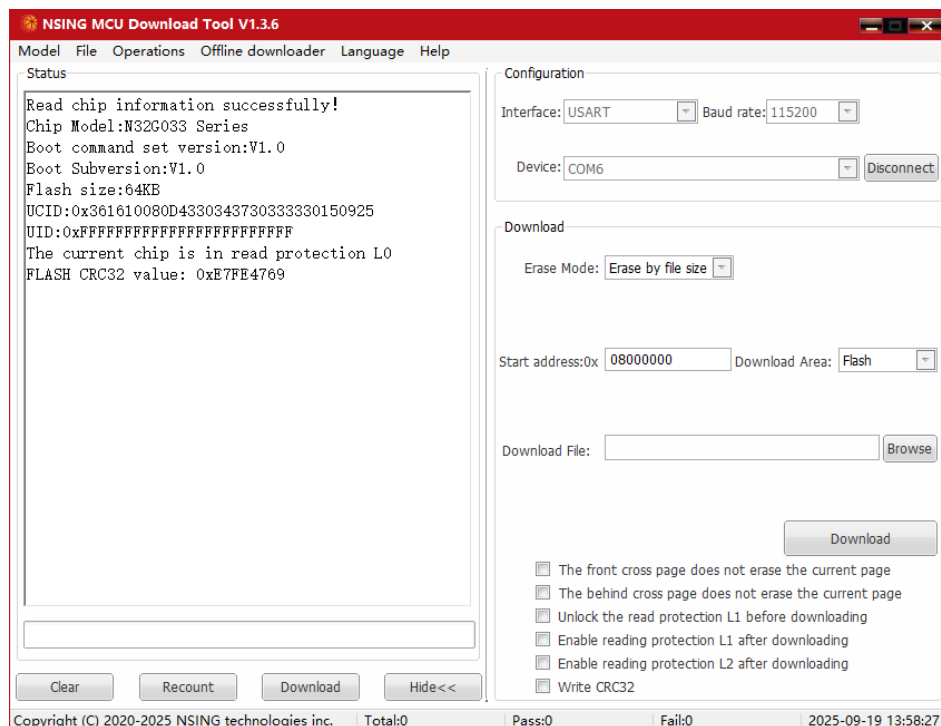


Figure 7-2 Device connection succeeded

### 7.1.3 Select download file

**Download file:** Optional bin \ hex \ enc files. It is recommended to download files with a size not less than page size or not less than 2k;

Click "Browse", select the file to download in the pop-up dialog box, double click the file, or click "Open", as shown below:

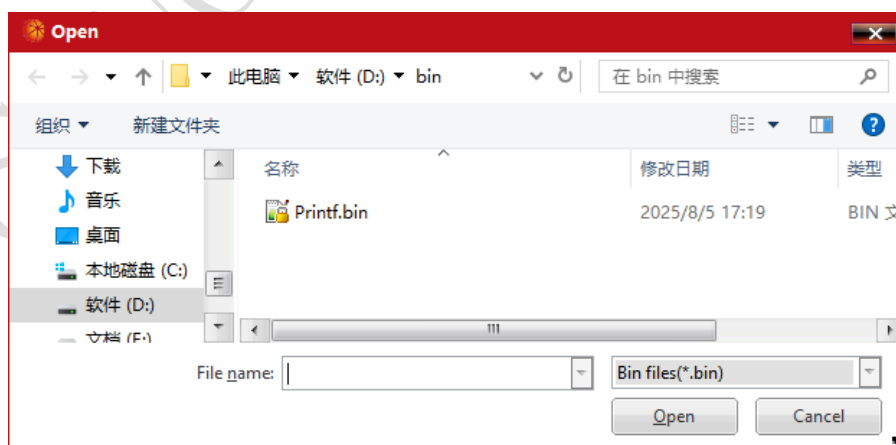


Figure 7-3 Selecting the download file

### 7.1.4 Download Parameter Configuration

Users can choose the erase mode and configuration before and after downloading based on their actual situation

**Erase mode:** erase by file size, full erase, no erase.

**Starting address:** The starting address of the download, default 0x08000000, cannot exceed the range of the download area, the starting address must be aligned with 16 bytes, and the starting address of the download area for different series of chips may be different. Please fill in according to the actual situation.

**Note: N32G003 series, the first 3K is BOOT storage area:**

**FLASH area 0x0800C00~0x08003FFF/0x080075FF**

**Download Area:** For series chips with multiple download areas, if only the FLASH area is supported for download, the download area will not be displayed; According to different series of chips, different download areas are displayed. Selecting different download areas will display the starting address of the corresponding area, and the starting address and download range cannot exceed the range of the currently selected area. The specific scope of the area can be found in the user manual.

1. N32H78X\_H76X series:

ITCM area: 0x00000000~0x000FFFFF,

AXISRAM area: 0x24000000~0x2411FFFF,

AHBSRAM area: 0x30000000~0x30057FFF,

FLASH area: 0x150000000~0x151DFFFF/0x153DFFFF

2. N32G05X series:

FLASH area: 0x08000000~0x0801FFFF

DATA FLASH area: 0x1FFF1000~0x1FFF2FFF

SRAM area: 0x20001000~0x20003FFF

3. N32G033 series:

FLASH area: 0x08000000~0x0800FFFF

SRAM area: 0x20000500~0x200017FF

#### 4. N32H47X\_H48X series:

FLASH area: 0x08000000~0x0803FFFF/0x0807FFF/0x0807FFF

SRAM area: 0x2000A000~0x20030FFF

**The front cross page does not erase the current page** ☐ If the download starting address is not aligned with the page, unchecking it will default to erasing the current page where the starting address is located. Checking it will not erase it.

**The behind cross page does not erase the current page:** When the download end address is not page aligned, unchecking it will default to erasing the current page where the end address is located. Checking it will not erase the current page.

**Unlock the read protection L1 before downloading:** If checked, check whether the chip has enabled read protection level L1 before downloading. If yes, release L1 first. If not checked, do not process.

**Enable reading protection L1 after downloading:** Check to determine if the chip has enabled read protection level L1 after downloading. If not, enable L1. If not checked, do not process.

**Enable reading protection L2 after downloading:** Check to determine if the chip has enabled read protection level L2 after downloading. If not, enable L2. If not checked, do not process.

### 7.1.5 Start the download

After completing the above operations, you can click the "Download" button below to download the program. After the program is successfully downloaded, as shown in the following figure:

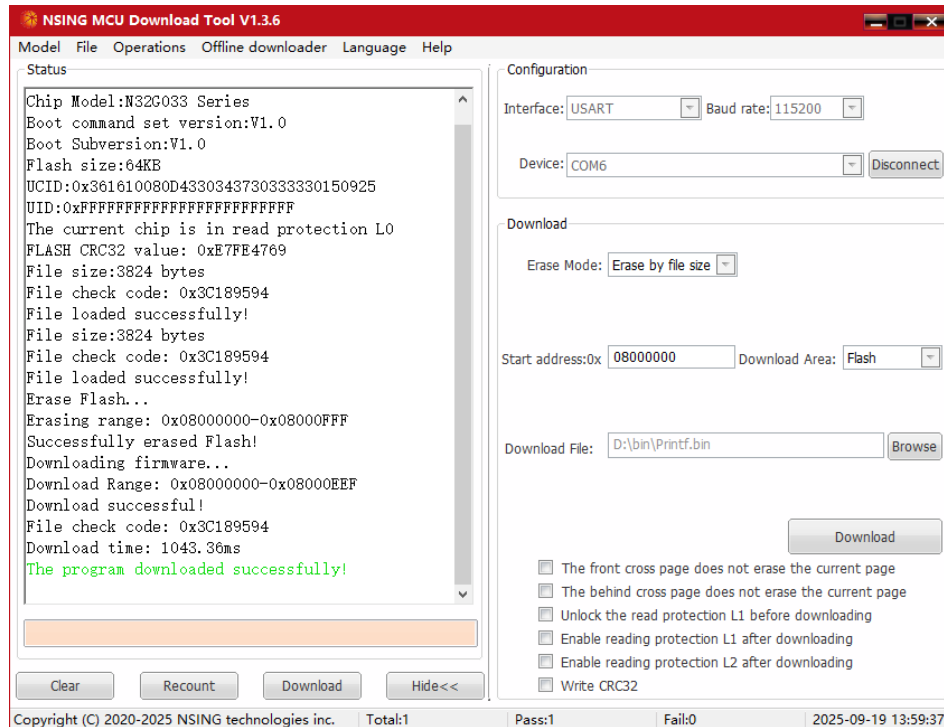


Figure 7-4 Program downloaded successfully

**NOTE:N32G003 Series chip,the first 3k is the BOOT storage area,the user area download address starting address is 0x08000C00!**

## 7.2 USB (DFU) program download

### 7.2.1 Select equipment

Connect the target chip and PC through USB cable, pull the target chip BOOT0 pin high, reset or power on the target chip, and then the target chip enters BOOT. Open the tool and check whether the current device can be enumerated (take N32H473 series chips as an example), as shown in the figure:



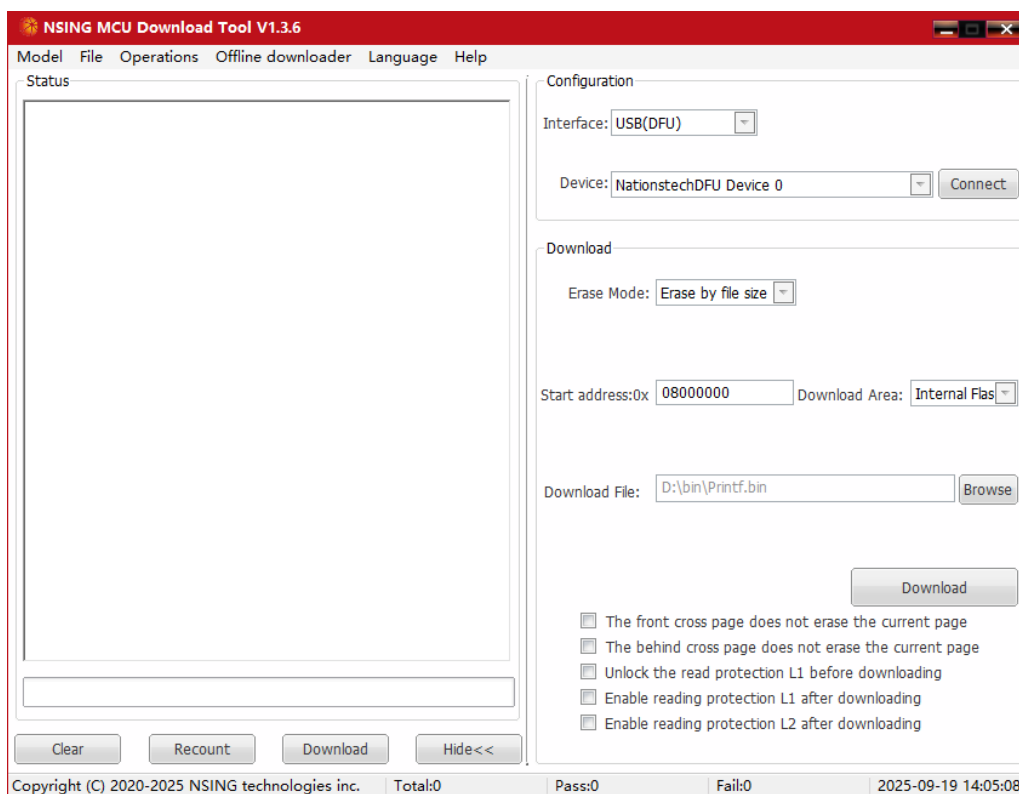


Figure 7-5 Selecting a device

## 7.2.2 Connected devices

Click "Connect Device", the target chip information will be printed.

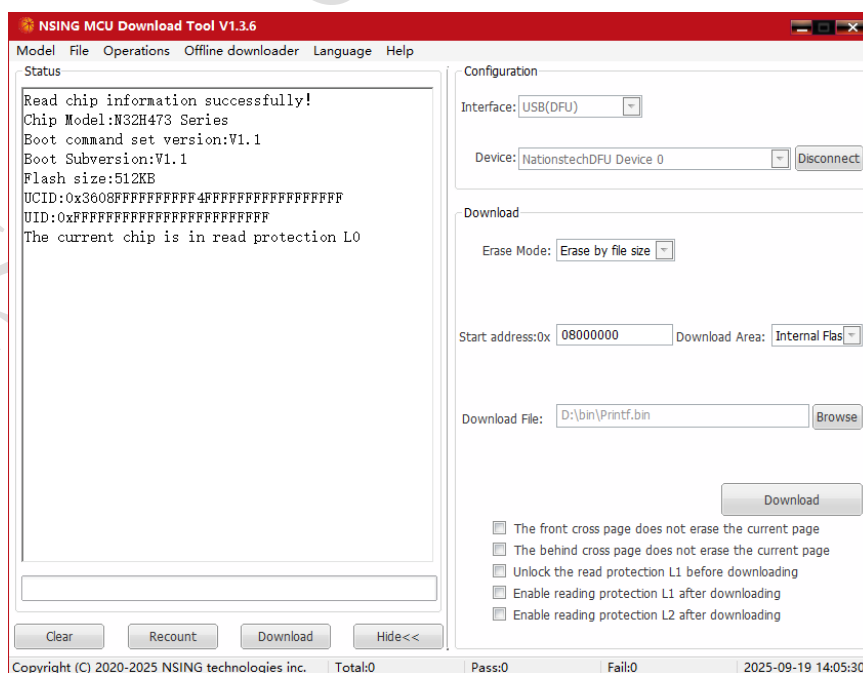


Figure 7-6 Connecting devices

### 7.2.3 Select download file

**Download file:** Optional bin \ hex \ enc files. It is recommended to download files with a size not less than page size or not less than 2k;

Click browse, select download file, and then click Open.

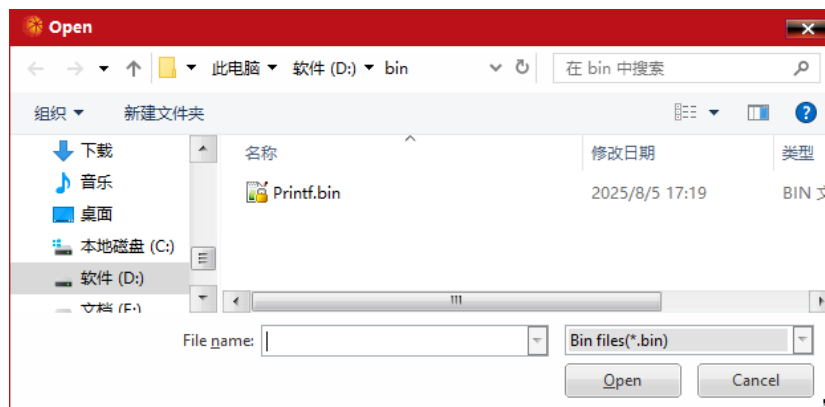


Figure 7-7 Selecting a file

### 7.2.1 Download Parameter Configuration

Users can choose the erase mode and configuration before and after downloading based on their actual situation

**Erase mode:** erase by file size, full erase, no erase.

**Starting address:** The starting address of the download, default 0x08000000, cannot exceed the range of the download area, the starting address must be aligned with 16 bytes, and the starting address of the download area for different series of chips may be different. Please fill in according to the actual situation.

**Note: N32G003 series, the first 3K is BOOT storage area:**

**FLASH area 0x0800C00~0x08003FF/0x080075FF**

**Download Area:** For series chips with multiple download areas, if only the FLASH area is supported for download, the download area will not be displayed; According to different series of chips, different download areas are displayed. Selecting different download areas will display the starting address of the corresponding area, and the starting address and download range cannot exceed the range of the currently selected area. The specific scope of the area can be found in the

user manual.

1. N32H78X\_H76X series:

ITCM area: 0x00000000~0x000FFFFF,

AXISRAM area: 0x24000000~0x2411FFFF,

AHBSRAM area: 0x30000000~0x30057FFF,

FLASH area: 0x150000000~0x151DFFFF/0x153DFFFF

2. N32G05X series:

FLASH area: 0x08000000~0x0801FFFF

DATA FLASH area: 0x1FFF1000~0x1FFF2FFF

SRAM area: 0x20001000~0x20003FFF

3. N32G033 series:

FLASH area: 0x08000000~0x0800FFFF

SRAM area: 0x20000500~0x200017FF

4. N32H47X\_H48X series:

FLASH area: 0x08000000~0x0803FFFF/0x0807FFF/0x0807FFF

SRAM area: 0x2000A000~0x20030FFF

**The front cross page does not erase the current page:** If the download starting address is not aligned with the page, unchecking it will default to erasing the current page where the starting address is located. Checking it will not erase it.

**The behind cross page does not erase the current page:** When the download end address is not page aligned, unchecking it will default to erasing the current page where the end address is located. Checking it will not erase the current page.

**Unlock the read protection L1 before downloading:** If checked, check whether the chip has enabled read protection level L1 before downloading. If yes, release L1 first. If not checked, do not process.

**Enable reading protection L1 after downloading:** Check to determine if the chip has enabled read protection level L1 after downloading. If not, enable L1. If not checked, do not process.

**Enable reading protection L2 after downloading:** Check to determine if the chip has enabled

read protection level L2 after downloading. If not, enable L2. If not checked, do not process.

## 7.2.2 Start the download

After completing the above operations, you can click the "Download" button below to download the program. After the program is successfully downloaded, as shown in the following figure:

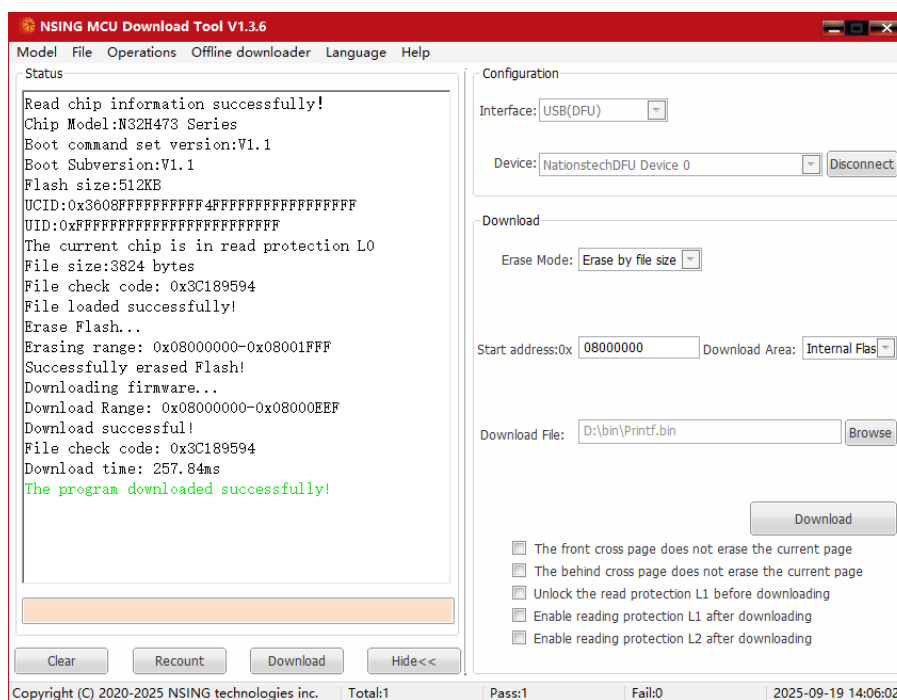


Figure 7-8 Downloading the file successfully

## 7.3 SWD(CMSIS-DAP) program download

### 7.3.1 Select equipment

Connect the target chip and PC through USB cable, and the target chip does not need to enter the boot. Open the tool and confirm whether the current device can be enumerated (take N32H473 series chip as an example), as shown in the figure:

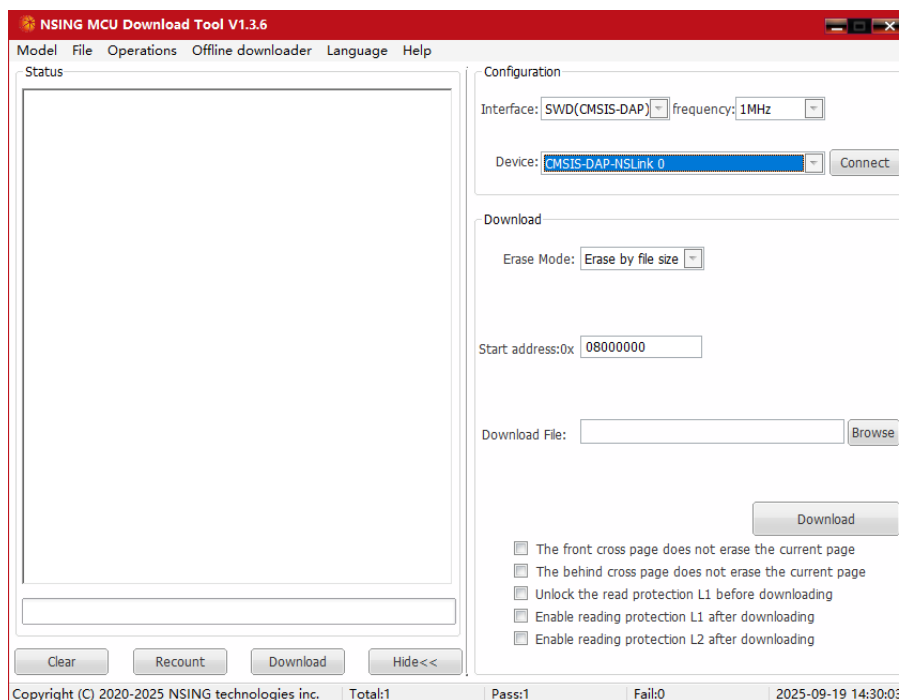


Figure 7-9 Selecting a device

### 7.3.2 Connected devices

After selecting the appropriate frequency, click "connect device", and the target chip information will be printed if the connection is successful.

Note: at present, NS Link Pro equipment only supports frequencies of 200kHz, 500KHz, 1MHz, 2MHz and 5MHz. If the target chip is at the read protection level L1 or L2, the connection may fail or the acquisition of chip information may fail. You can try to interpret the protection and then connect the device

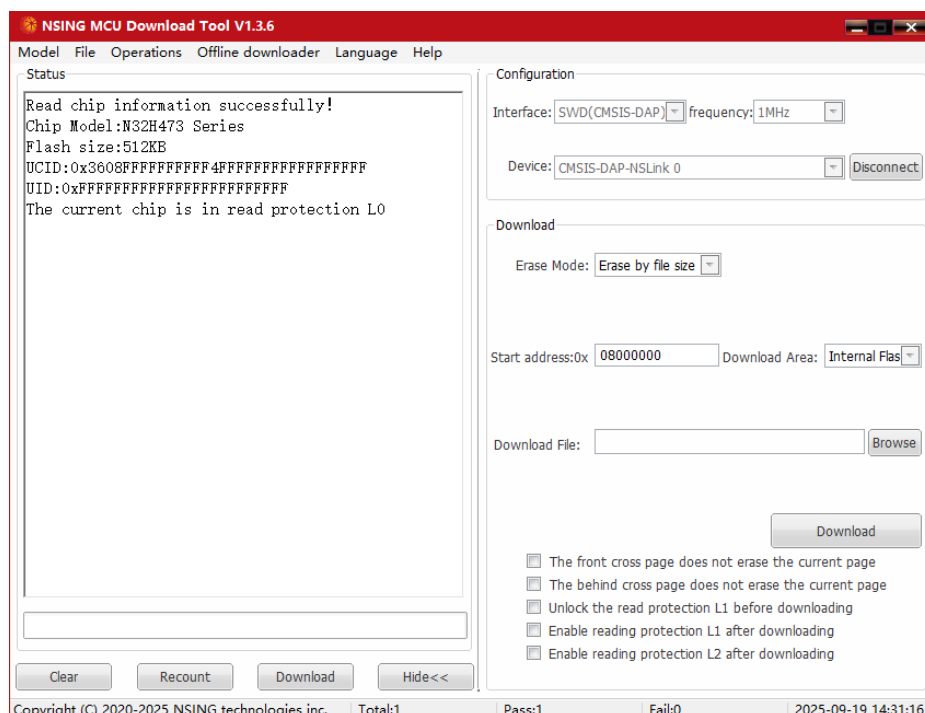


Figure 7-10 Connecting devices

### 7.3.3 Select download file

**Download file:** Optional bin \ hex files. It is recommended to download files with a size not less than page size or not less than 2k

Click browse, select download file, and then click Open.

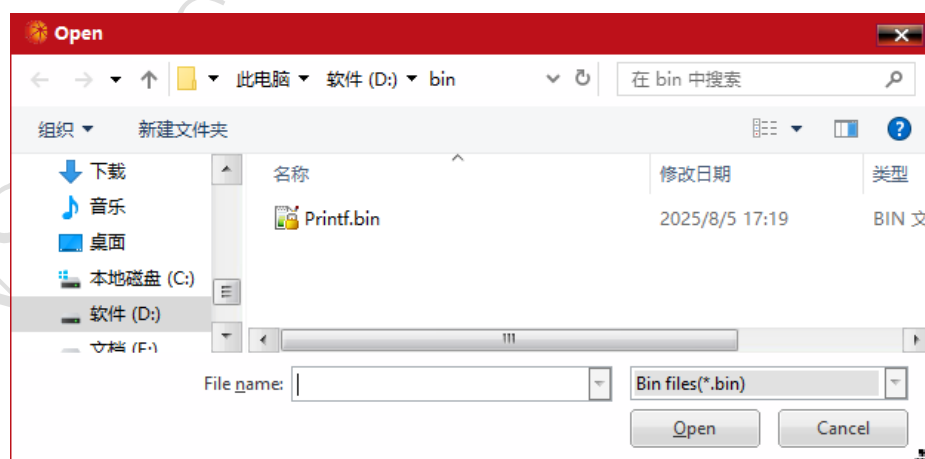


Figure 7-11 Selecting a file

### 7.3.4 Download Parameter Configuration

Users can choose the erase mode and configuration before and after downloading based on their

actual situation

**Erase mode:** erase by file size, full erase, no erase.

**Starting address:** The starting address of the download, default 0x08000000, cannot exceed the range of the download area, the starting address must be aligned with 8 bytes, and the starting address of the download area for different series of chips may be different. Please fill in according to the actual situation.

**Download Area:** For series chips with multiple download areas, if only the FLASH area is supported for download, the download area will not be displayed; According to different series of chips, different download areas are displayed. Selecting different download areas will display the starting address of the corresponding area, and the starting address and download range cannot exceed the range of the currently selected area. The specific scope of the area can be found in the user manual.

1. N32H78X\_H76X series:

ITCM area: 0x0000000~0x000FFFFF,

AXISRAM area: 0x24000000~0x2411FFFF,

AHBSRAM area: 0x30000000~0x30057FFF,

FLASH area: 0x15000000~0x151DFFFF/0x153DFFFF

2. N32G05X series:

FLASH area: 0x08000000~0x0801FFFF

DATA FLASH area: 0x1FFF1000~0x1FFF2FFF

SRAM area: 0x20001000~0x20003FFF

3. N32G033 series:

FLASH area: 0x08000000~0x0800FFFF

SRAM area: 0x20000500~0x200017FF

4. N32H47X\_H48X series:

FLASH area: 0x08000000~0x0803FFFF/0x0807FFF/0x0807FFF

SRAM area: 0x2000A000~0x20030FFF

**The front cross page does not erase the current page:** If the download starting address is not

aligned with the page, unchecking it will default to erasing the current page where the starting address is located. Checking it will not erase it.

**The behind cross page does not erase the current page:** When the download end address is not page aligned, unchecking it will default to erasing the current page where the end address is located. Checking it will not erase the current page.

**Unlock the read protection L1 before downloading:** If checked, check whether the chip has enabled read protection level L1 before downloading. If yes, release L1 first. If not checked, do not process.

**Enable reading protection L1 after downloading:** Check to determine if the chip has enabled read protection level L1 after downloading. If not, enable L1. If not checked, do not process.

**Enable reading protection L2 after downloading:** Check to determine if the chip has enabled read protection level L2 after downloading. If not, enable L2. If not checked, do not process.

### 7.3.5 Start the download

After completing the above operations, you can click the "Download" button below to download the program. After the program is successfully downloaded, as shown in the following figure:

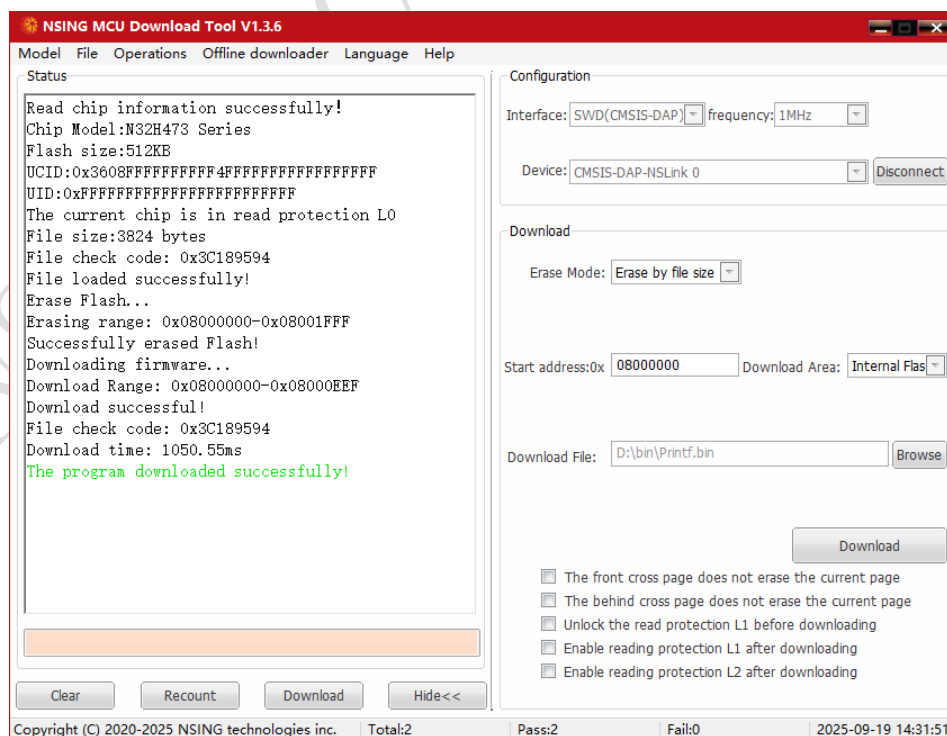


Figure 7-12 Downloading the file successfully



## 7.4 Document Production

### 7.4.1 Creating encrypted files

This operation is only applicable to configurable partitioned series chips and is used to generate encrypted files.

Select the key ID configured when configuring the partition to generate the corresponding encrypted file.

### 7.4.2 Creating Key Files

This operation is only applicable to N32H78x and N32H76x series chips and is used to generate random number keys, identity authentication keys, JTAG keys, and nonce files. One or more key files can be generated based on the input quantity. When the key encryption save is selected, the key will be encrypted to generate an encrypted key. Otherwise, a plaintext key will be generated. By default, it is saved to the Key folder in the tool directory, and supports self selection of the save path.

### 7.4.3 Creating Security Firmware Files

This operation is only applicable to N32H78x and N32H76x series chips and is used to generate security firmware files. Security firmware can only be downloaded to XSPI.

Start address: The starting address for downloading, default is 0x150000000, and the input range cannot exceed the XSPI area range.

Data file: The program file must contain security configuration information, that is, the first 4 bytes of the file must be "NSSF".

Nonce file: The nonce file generated when creating an encrypted file.

REK/IDKEY file: The random number key and authentication key generated when creating encrypted files.

Encryption type: optional encryption without binding or encryption binding

Opt: Select the corresponding option byte according to the requirements

Save Path: Default saved to the Firmware folder in the tool directory, supports self selected save path

#### **7.4.4 Creating Security Module Files**

This operation is only applicable to N32H78x and N32H76x series chips and is used to generate security module files.

Download address: The starting address for downloading, default is 0x150000000, and the input range cannot exceed the XSPI area range.

Program file: downloaded file data

Nonce file: The nonce file generated when creating an encrypted file.

Save Path: Default saved to the Firmware folder in the tool directory, supports self selected save path

### **7.5 Common Operation Instructions**

#### **7.5.1 Obtaining chip information**

This operation enables you to read the chip model, BOOT version, FLASH capacity, UCID, and UID. When the device is connected, you can click the "Get chip information" button in other operations, as shown in the picture below after the correct execution:

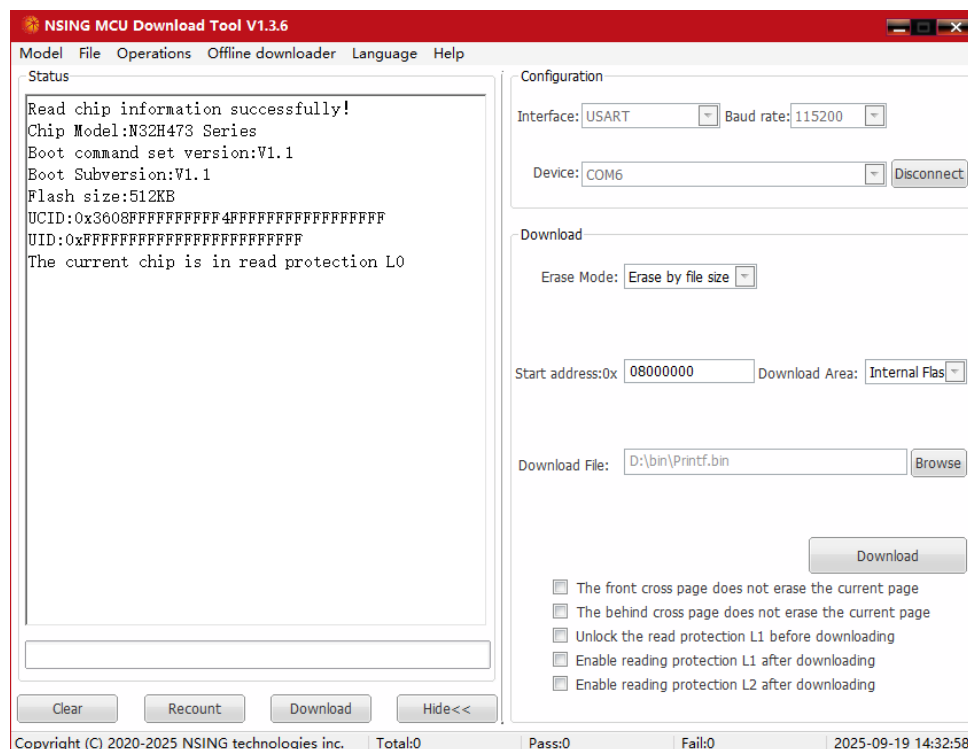


Figure 7-13 Obtaining chip information

## 7.5.2 Configuration partition

This operation is used to read or configure the size of the user1/2/3 partition. After the partition is configured, the partition is automatically sealed. The user1/2/3 partition can be configured only once. The software determines whether the NVR MMU partition has been configured (process variables or random delay are added to determine the NVR value).

The recommended configuration process is as follows:

1. If you need to divide two areas, configure USER3 (automatic sealing is complete). If you want to also seal USER1, configure USER1 again. The size of USER1 + USER3 must be the size of the entire FLASH;
2. To divide three zones, configure USER3 (automatic sealing is configured) and then USER2 (automatic sealing is configured). If you want to also seal USER1, configure USER1 again. The size of USER1 + USER2 + USER3 must be the size of the entire FLASH.

Click the menu of "Configure Partition" in advanced configuration at the upper left corner. In the pop-up dialog box, users can set the size, key ID(0-31), enable partition authentication and enable encrypted download as required, as shown below:

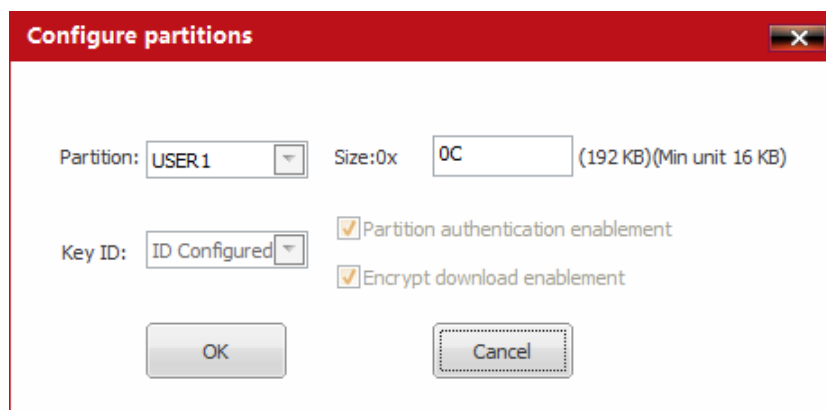


Figure 7-14 Configuring partitions

### 7.5.3 Partition download configuration

If the user has configured the partition, it needs to download the partition. Click the "Partition Download Configuration" menu bar of common operations in the upper left corner, and select the parameter configuration of the corresponding partition in the pop-up dialog box, as shown below:

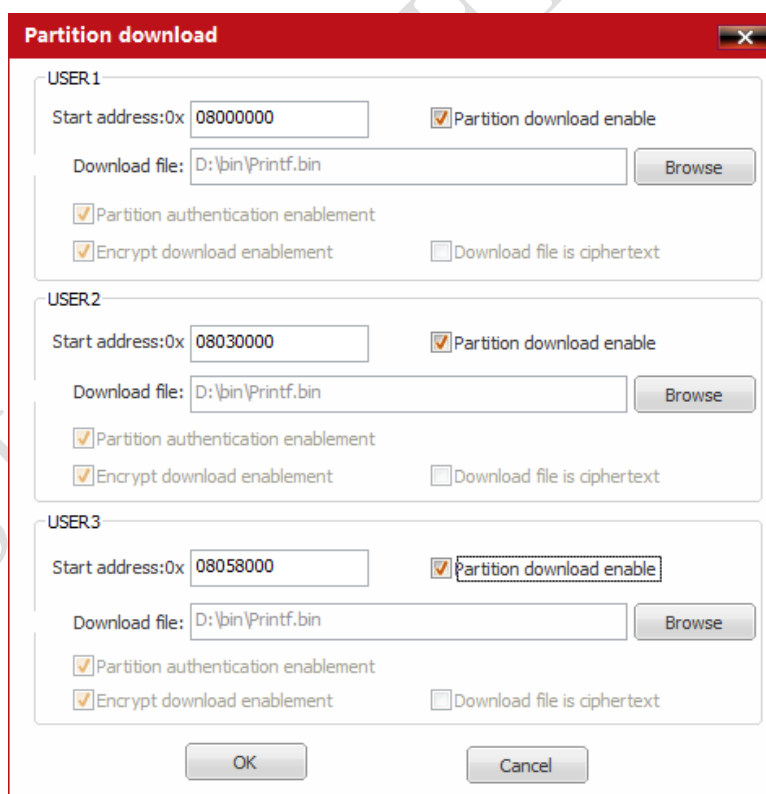


Figure 7-15 Partition download configuration

**Start address:** start address for downloading

**Download files:** Files that need to be downloaded

**Zone authentication and encrypted download:** If zone authentication and encrypted

download have been enabled for the corresponding zone, the check box is automatically displayed.

**Enable partition download:** indicates whether to download the partition. If check box is displayed, download the partition. If check box is displayed, download the partition will not be downloaded.

**The downloaded file is ciphertext:** Check box indicates that the downloaded file is encrypted. Otherwise, the downloaded file is not encrypted. If encrypted download is enabled and the downloaded file is not encrypted, the host encrypts the file before downloading it.

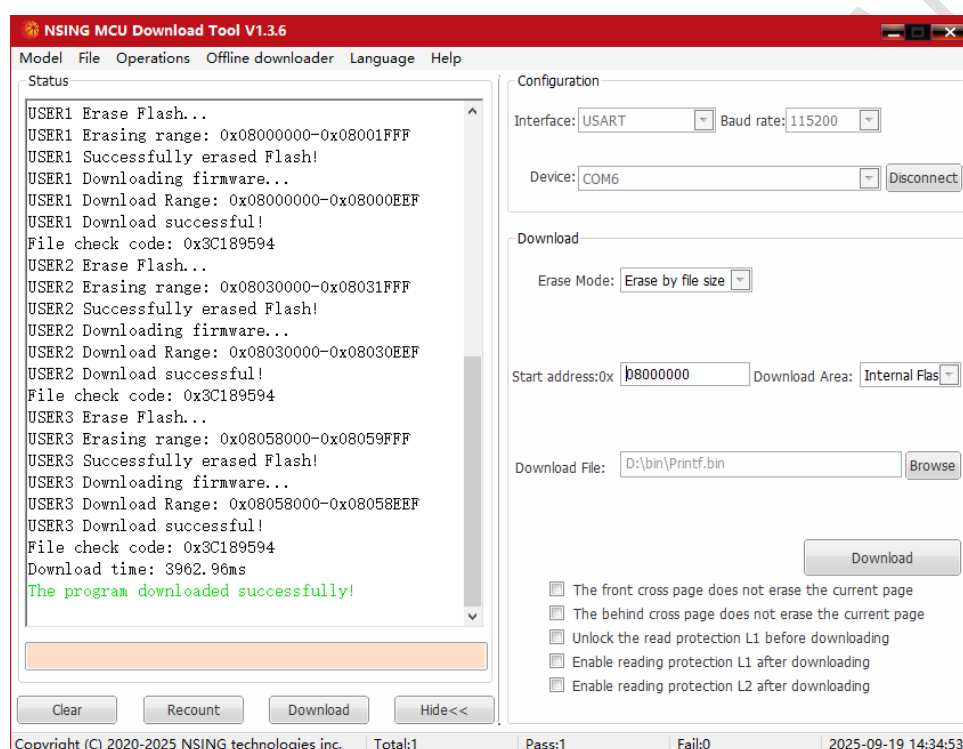


Figure 7-16 Partition downloaded successfully

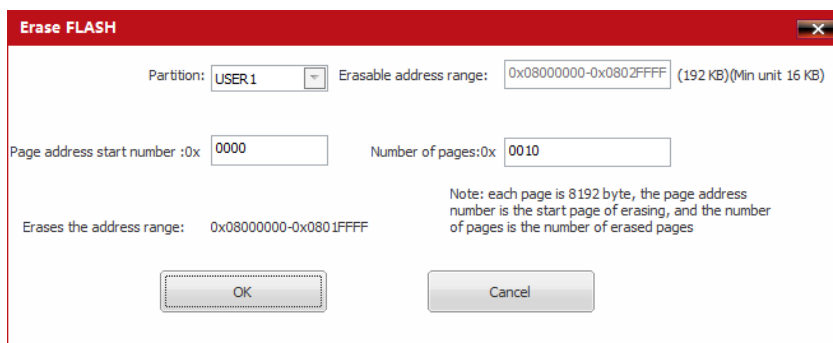
## 7.5.4 All erased

Erase the entire FLASH. Chips configured with partitions do not support full erase.

## 7.5.5 Page to erase

BOOT allows you to erase the FLASH on a page basis. The space that can be erased cannot exceed the entire FLASH space and at least one page can be erased. Click the "Erase sectors" button in other operations. In the FLASH erase dialog box that pops up, the user fills in the page address number and page number to be erased according to the address range of the partition. As shown

below:



**Erase FLASH**

Partition:  Erasable address range:  (192 KB)(Min unit 16 KB)

Page address start number :0x  Number of pages:0x

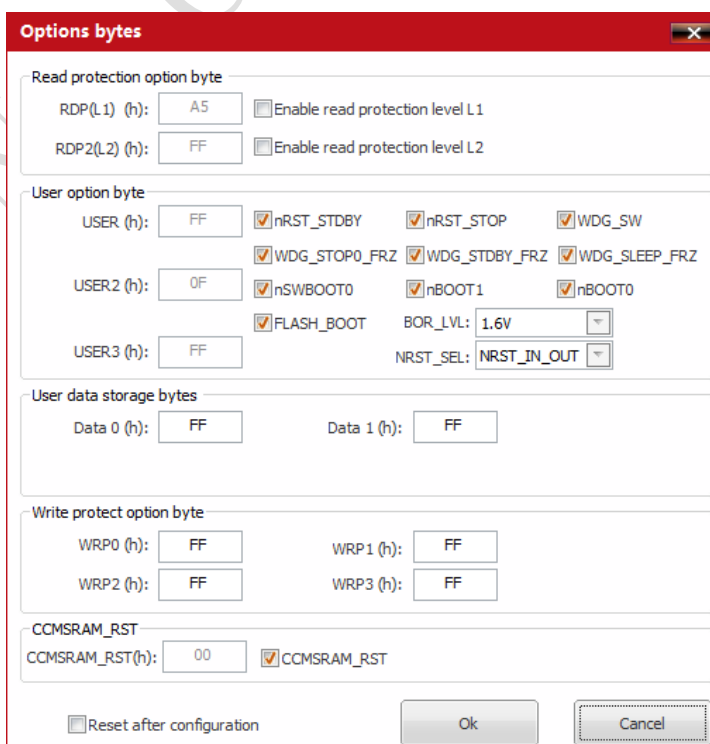
Erases the address range: 0x08000000-0x0801FFFF

Note: each page is 8192 byte, the page address number is the start page of erasing, and the number of pages is the number of erased pages

Figure 7-17 Erasing FLASH

### 7.5.6 Configuration option byte

This operation is used for option byte read and write (including read protection level, FLASH page write protection, data0/1 configuration, and USER configuration).When a partition is configured, BOOT does not allow you to change the read protection level from L1 to L0 because mass erase!Click the button of "Configuration Option Byte" in other operations, and in the pop-up dialog, the user can set the corresponding byte data as required, The byte options for different series of chips may vary, please refer to the user manual for details, Taking the N32H473 and N32H78X\_H76X series as an example, as shown in the figure:



**Options bytes**

**Read protection option byte**

RDP(L1) (h):  ☐ Enable read protection level L1

RDP(L2) (h):  ☐ Enable read protection level L2

**User option byte**

USER (h):  ☒ nRST\_STDBY ☒ nRST\_STOP ☒ WDG\_SW

☒ WDG\_STOP0\_FRZ ☒ WDG\_STDBY\_FRZ ☒ WDG\_SLEEP\_FRZ

USER2 (h):  ☒ nSWBOOT0 ☒ nBOOT1 ☒ nBOOT0

☒ FLASH\_BOOT BOR\_LVL:

USER3 (h):  NRST\_SEL:

**User data storage bytes**

Data 0 (h):  Data 1 (h):

**Write protect option byte**

WRP0 (h):  WRP1 (h):

WRP2 (h):  WRP3 (h):

**CCMSRAM\_RST**

CCMSRAM\_RST(h):  ☒ CCMSRAM\_RST

☐ Reset after configuration

Figure 7-25 N32H473 option bytes

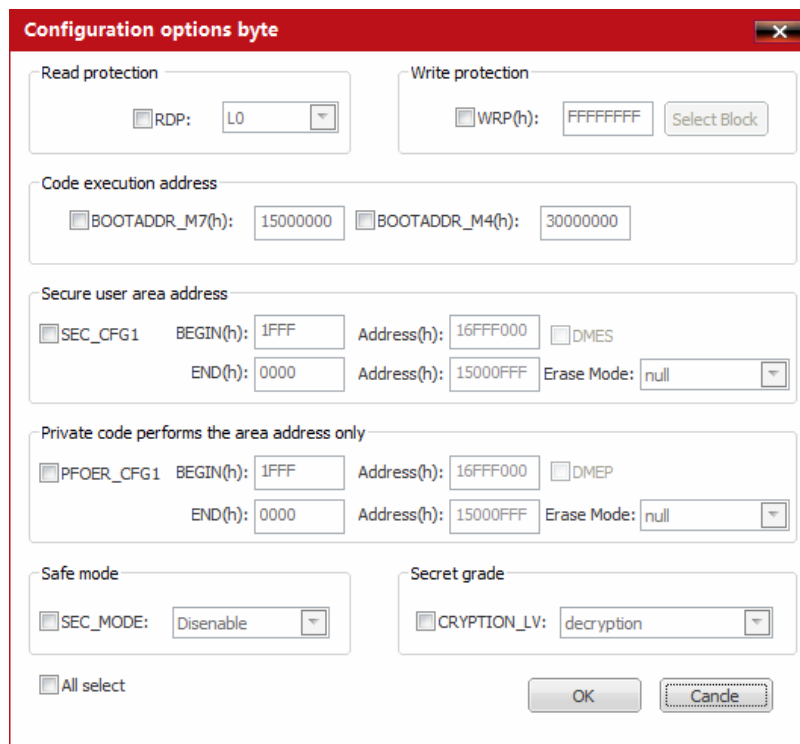


Figure 7-26 . N32H78X\_H76X option bytes

Note: The N32H78X\_H76X series 1A version currently does not support the configuration of SEC\_CFG1, PFOER\_CFG1, SEC-PODE, and CRYPTION-LV.

### 7.5.7 Read protection

If the read protection level L0 is enabled, you can set the read protection level to L1 or L2.

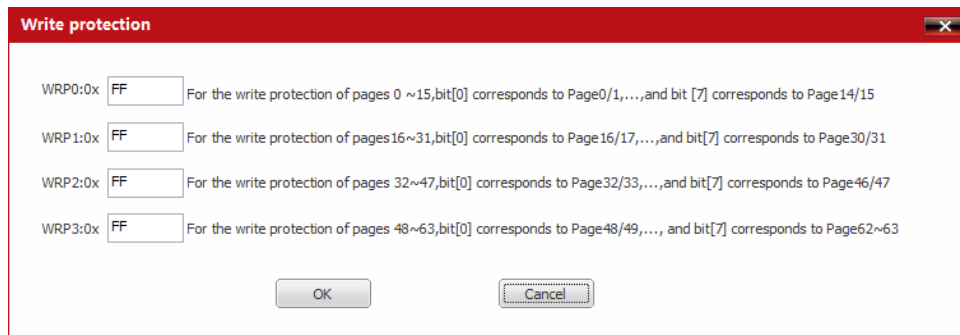
If the read protection level L1 is enabled, you can lower the read protection level to L0.

If the read protection level L2 is enabled, the read protection level cannot be lowered to L0.

If partitions have been configured, the read protection level cannot be changed from L1 to L0

### 7.5.8 Write protection

Write protection can be configured for all pages in the Flash main storage area to prevent accidental write operations caused by program crashes or electrical interference. Write protection can be configured by setting WRP0~3 in the option byte block. The basic unit of write protection varies depending on the different series of chips. Please refer to the user manual for each series of chips for details.



**Write protection**

WRP0:0x  For the write protection of pages 0 ~15,bit[0] corresponds to Page0/1,...,and bit [7] corresponds to Page14/15

WRP1:0x  For the write protection of pages16~31,bit[0] corresponds to Page16/17,...,and bit[7] corresponds to Page30/31

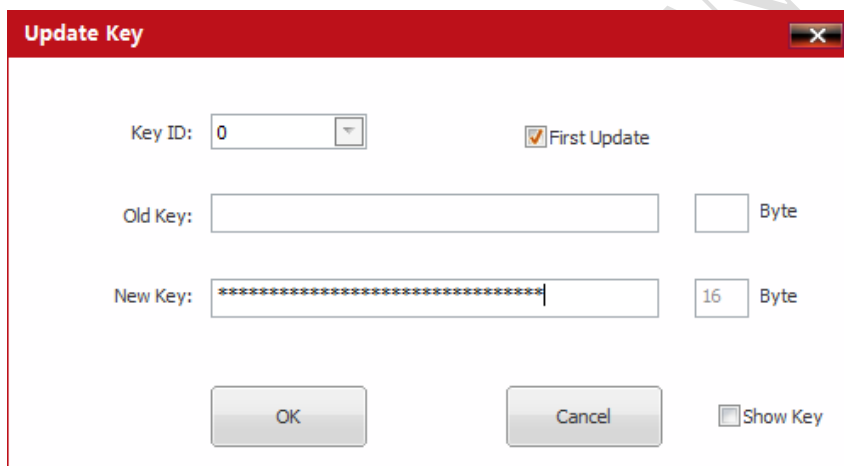
WRP2:0x  For the write protection of pages 32~47,bit[0] corresponds to Page32/33,...,and bit[7] corresponds to Page46/47

WRP3:0x  For the write protection of pages 48~63,bit[0] corresponds to Page48/49,..., and bit[7] corresponds to Page62~63

### 7.5.9 Update the key

This operation is used to update the encryption download key and partition authentication key.

To update the key, enter the old key first, as shown in the following figure:



**Update Key**

Key ID:  ☐ First Update

Old Key:

New Key:

☐ Show Key

Figure 7-19 Updating a key

### 7.5.10 reset

This operation is used to reset the BOOT program. After the reset is successful, the tool will automatically reconnect, as shown in the following figure:



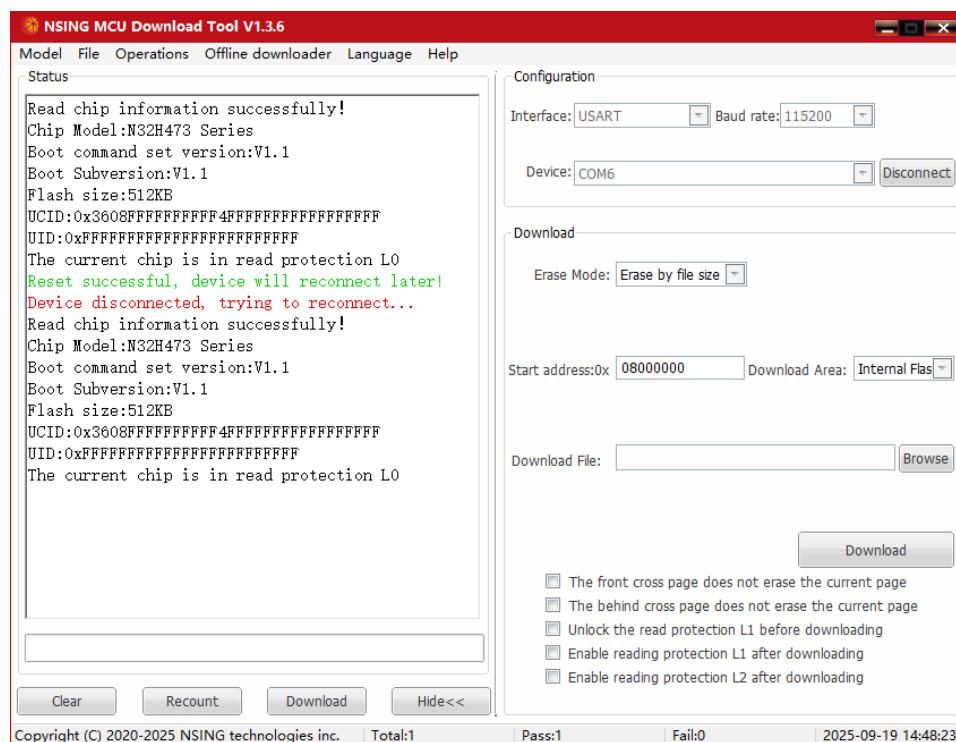


Figure 7-20 reset

### 7.5.11 App go

This operation is used to jump to the FLASH after BOOT downloads the application program. USER1 Reset the address of the program entrance (0x0800\_0000). (After the user partition is enabled, the jump command is not recommended. Because the interrupt direction table start address may not be set again, the user program cannot handle interrupts properly.

### 7.5.12 Flash seal

This operation is only applicable to N32G05x series chips and seals FLASH (main flash and data flash).

### 7.5.13 SRAM jump

This operation is only applicable to N32G05x series chips and is used to jump to the reset program entry address after downloading the SRAM program. The SRAM address is 0x2000\_0000~0x2000\_3FFF, 16KB, 32 pages.

### **7.5.14 Setting JTAG Mode**

This operation is only applicable to N32H78x and N32H76x series chips and is used to modify the JTAG mode. You can choose to enable or disable the JTAG mode. If the key has not been modified, check the option to use the default key. If the key has been modified, select the modified key.

### **7.5.15 Setting JTAG Key**

This operation is only applicable to N32H78x and N32H76x series chips and is used to modify JTAG keys.

### **7.5.16 Set OTP**

This operation is only applicable to N32H78x and N32H76x series chips and is used to modify OTP,

The OTP data range refers to the product manual.

## **8 Offline project download**

Offline Download Files can be downloaded through an offline download device. SWD and USART(serial port) are supported. Users can set up offline project files through the upper computer and choose the communication interface to download according to their own needs. After the user loads the project file to the offline downloader through the upper computer, the offline downloader can be detached from the PC for offline download.

### **8.1 Common Operation Instructions**

#### **8.1.1 Parameter Settings**

This page is mainly to set the control parameters of the downloader itself and the machine. Click the "Save parameter" button, and the parameters will be saved to the offline downloader, as shown in the picture:

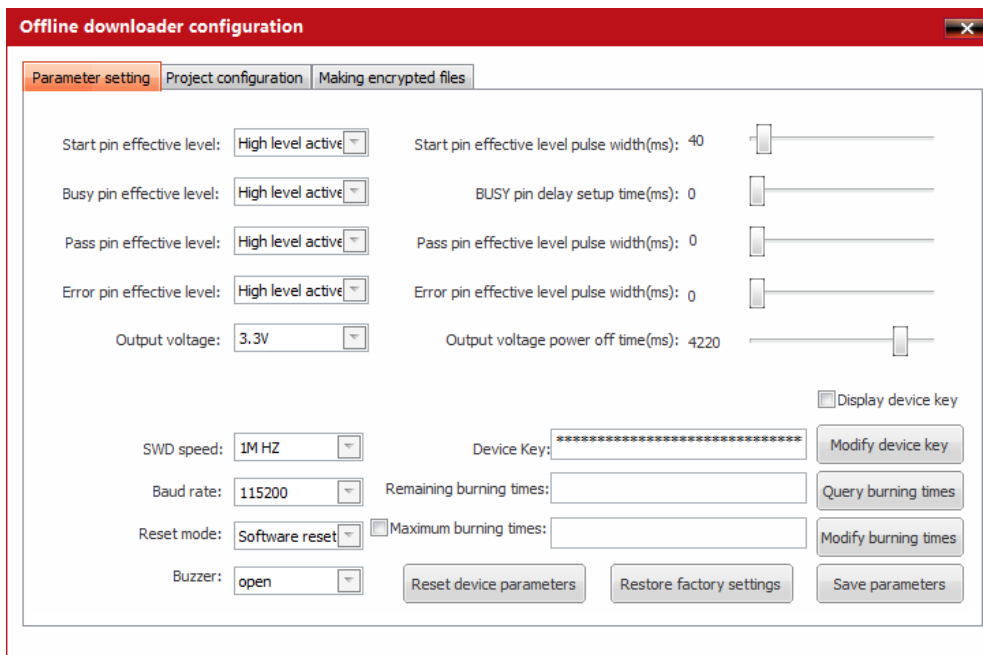


Figure 8-1 Parameter Settings

#### 8.1.1.1 Machine control signal setting

Note: Refer to section 8.6 for detailed timing requirements

##### ■ **START signal (machine burning START signal) :**

###### ➤ **START Pin effective level:**

- When set to high level effective, the downloader waits to receive high level pulse signal as the start signal.
- When set to low level effective, the downloader waits to receive low level pulse signal as the start signal.

###### ➤ **START pin effective level pulse width: 50~1000ms**

##### ■ **BUSY signal (machine burning BUSY signal) :**

###### ➤ **BUSY pin effective level:**

- When set to high active, the downloader is at high level during the download.
- When set to low active, the downloader is at high level during the download.

###### ➤ **BUSY pin chattering time: 0-1000ms, refers to the time between the download receives the start signal and sets the BUSY pin as the effective level chattering time.**

##### ■ **PASS signal (machine burning success signal) :**

###### ➤ **PASS pin effective level:**

- a) When it is set to high level effective and the pulse width of PASS effective level is equal to 0, the downloader outputs high level after downloading successfully.
- b) When set to high level effective, and the pulse width of PASS effective level is not 0, the downloader outputs high level pulse after downloading successfully.
- c) When it is set to low level effective and the pulse width of PASS effective level is equal to 0, the downloader outputs low level after downloading successfully.
- d) When it is set to low level effective and the pulse width of PASS effective level is not 0, the downloader outputs low level pulse after downloading successfully.

➤ **Pulse width of effective level of PASS pin:** 0-1000ms. When it is 0, it continuously outputs effective level; when it is not 0, it outputs effective level pulse.

■ **ERROR signal (burning failure signal of machine) :**

➤ **ERROR pin effective level:**

- e) When set to high level effective and ERROR effective level pulse width is equal to 0, the downloader outputs high level after downloading successfully.
- f) When set to high level effective and ERROR effective level pulse width is not 0, the downloader outputs high level pulse after downloading successfully.
- g) When set to low level effective and ERROR effective level pulse width is equal to 0, the downloader outputs low level after downloading successfully.
- h) When set to low level effective and ERROR effective level pulse width is not 0, the downloader outputs low level pulse after downloading successfully.

➤ **ERROR pin effective level pulse width:** 0-1000ms, when 0, continuously output effective level, when not 0, output effective level pulse.

■ **VT output voltage:**

- **VT output voltage:** when the downloader receives the start signal, VT turns on the voltage output and turns off after downloading
- a) No output.
  - b) 3.3 V output.

c) 5 v output.

➤ **Hold time of output voltage after downloading:**

- a) 0: turns off the VT power output immediately after the device is successfully downloaded to prevent power-on chip downloading.
- b) Non-0: Indicates that the VT voltage output is disabled after a period of time.
- c) Unlimited: Indicates that the VT output voltage remains after the download is complete and the VT power output is not turned off.

In particular, when the downloader receives the START signal to START the download, the power will be off immediately after the download is complete. This configuration is invalid. This configuration is invalid when the downloader is in continuous download mode (dip switch is in continuous download mode).

#### 8.1.1.2 Device Parameter Setting

■ **Download speed Settings**

➤ **SWD speed:**

The SWD transmission speed of the download can be selected as 100KHz, 200K, 500KHz, 1MHz, 2MHz and 5MHz

➤ **Baud rate:**

Set the baud rate for UART downloading

■ **Reset mode:** it is used to reset and start after the download is complete.

- Software reset
- Hardware pins reset

■ **Buzzer:** Buzzer enable option

■ **Modify device key:** Modify the key of the downloader

■ **Restore factory Settings:** Clear all offline download parameters and storage data to restore the factory default values.

■ **Save parameters:** Save the parameters configured above to the downloader

### 8.1.2 Offline Project Configuration

This page is mainly used to display and make offline project files, as shown in the figure

below:

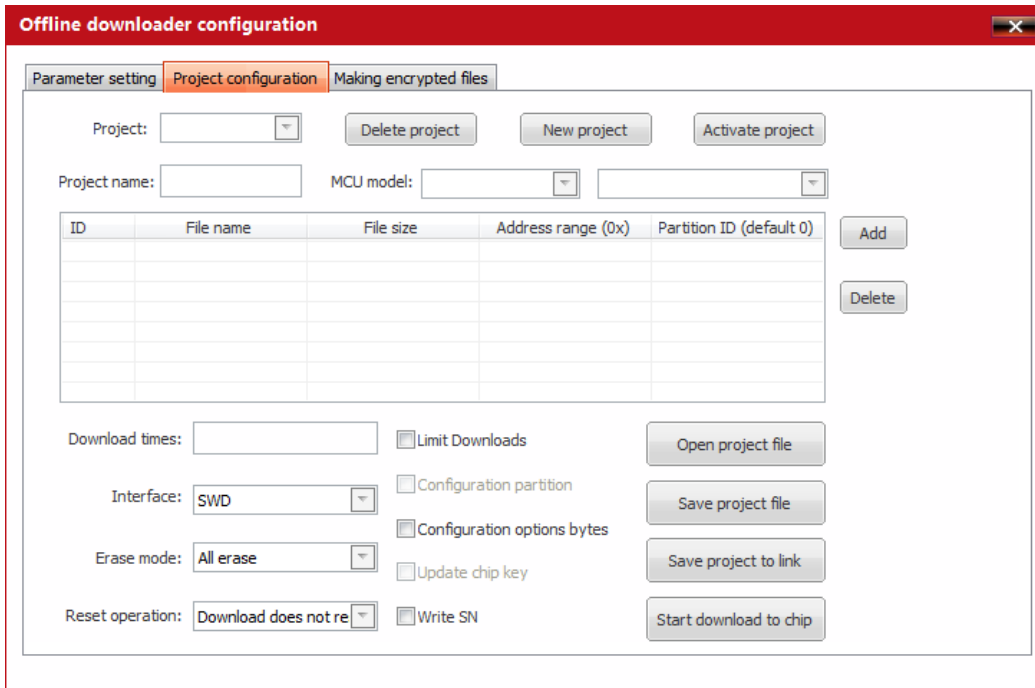
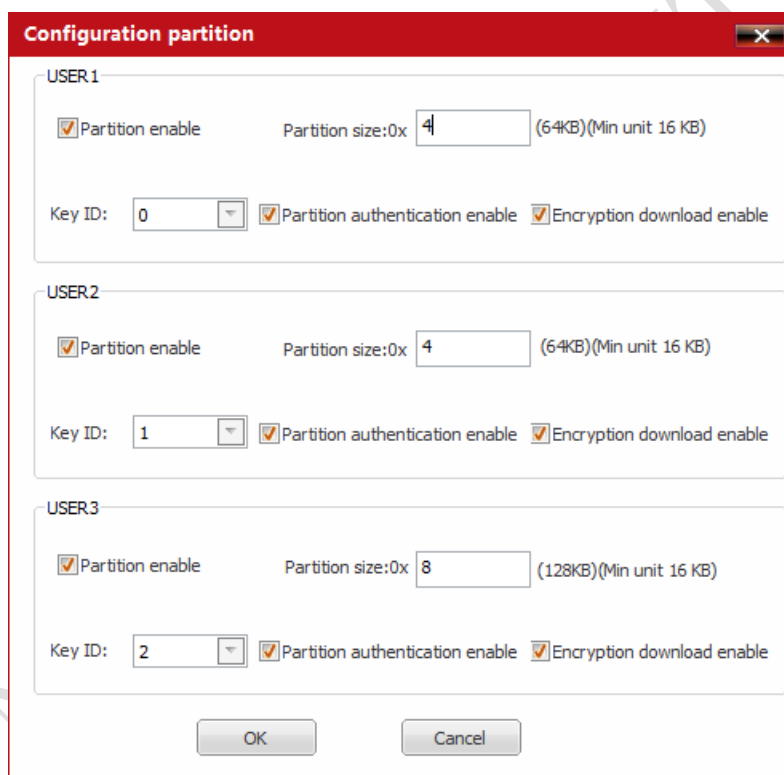


Figure 8-2 Project configuration

- **Project name:** User-defined project name when creating a project. The value can contain a maximum of 32 bytes.
- **MCU model:** When a new project is created, only the current series of MCU target boards are allowed to download when the option byte configuration is selected.
- **Add or Delete files:** When creating a project, add or delete files to be downloaded. The file format can be bin, HEX, or ENC. A maximum of eight files can be downloaded. The total size of the files to be added cannot be larger than the Flash size of the selected chip. If the configuration partition is selected, select the partition to download the file.
- **Limit download times/Download times:** Sets the maximum number of downloads supported by the download device
- **Communication interface:** Select the interface used for downloading
  - SWD
  - UART interface
- **Erase mode:**
  - SWD interface download
    - a) It's erased

- b) Erase according to file
- Download the UART interface
  - a) Partition erase
  - b) Erase according to file
- **Reset operation:** You can choose whether to reset after the download
- **Partition configuration:** Currently, only UART communication interfaces are supported, including partition size, partition download enablement, key ID, partition authentication enablement, and encrypted download enablement, as shown in the figure:



**Configuration partition**

**USER 1**

☒ Partition enable      Partition size: 0x  (64KB)(Min unit 16 KB)

Key ID:   ☒ Partition authentication enable ☒ Encryption download enable

**USER 2**

☒ Partition enable      Partition size: 0x  (64KB)(Min unit 16 KB)

Key ID:   ☒ Partition authentication enable ☒ Encryption download enable

**USER 3**

☒ Partition enable      Partition size: 0x  (128KB)(Min unit 16 KB)

Key ID:   ☒ Partition authentication enable ☒ Encryption download enable

Figure 8-3 Configuring partitions

- ✧ **Enable partition download:** Indicates whether to configure the current partition
- ✧ **Partition size:** indicates the size of the configuration partition.

Note:

For the N32G(WB)45x\_FR series, N32G(L) 43X and N32L40X series, USER1 of the chip can be set to a size of 0x00. Select the encryption or authentication mode, indicating that USER1 does not seal and only uses the encryption or authentication function.

- ✧ **Key ID:** 0x00-0x1F ID of the encryption download/Partition authentication key index
- ✧ **Zone authentication Enable:** Indicates whether to enable zone authentication.  
Once zone authentication is enabled for the target chip, it cannot be undone and is an irreversible operation.
- ✧ **Encrypted download enable:** indicates whether to enable encrypted download.  
Once partition authentication is enabled on the target chip, the subsequent operations cannot be undone. Therefore, only the key value of the target chip can be changed.

#### Recommended partition configuration process:

1. If you need to divide two areas, configure USER3 (automatic sealing is complete).If you want to also seal USER1, configure USER1 again.The size of USER1 + USER3 must be the size of the entire FLASH;
2. To divide three zones, configure USER3 (automatic sealing is configured) and then USER2 (automatic sealing is configured).If you want to also seal USER1, configure USER1 again.The size of USER1 + USER2 + USER3 must be the size of the entire FLASH.

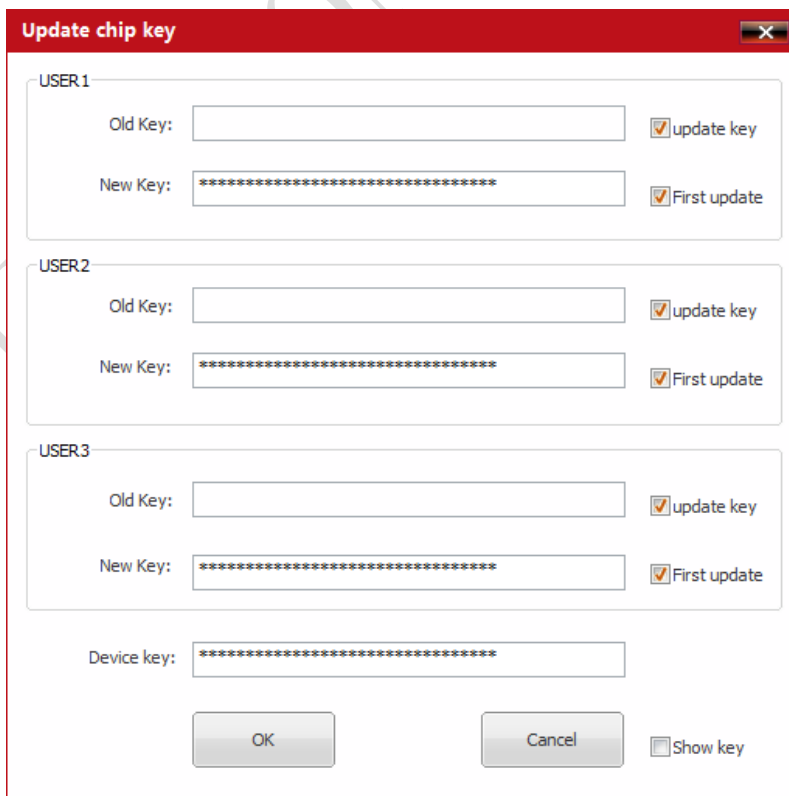
**It is recommended that users perform encryption authentication operations according to the following:**

Encrypted Authentication Operation				
	No partition authentication operation is performed during download, and data is not encrypted	No partition authentication operation is performed during download, and data is encrypted	The partition authentication operation is performed during download, and the data is not encrypted	Partition authentication operation and data encryption during download
<b>Key not</b>	1. Uncheck the partition	1. Uncheck the partition	1. Check the partition	1. Check the partition



<b>updated after factory (default key)</b>	authentication enable 2. Uncheck Encrypted Download Enable	authentication enable 2. Check the encrypted download enable	authentication enable 2. Uncheck Encrypted Download Enable	authentication enable 2. Check encryption and then enable
<b>The key has been updated since the factory</b>	1. Uncheck the partition authentication enable 2. Uncheck Encrypted Download Enable	1. Uncheck the partition authentication enable 2. Check the encrypted download enable 3. Check the update key	1. Check the partition authentication enable 2. Uncheck Encrypted Download Enable 3. Check the update key	1. Check the partition authentication enable 2. Check the encryption and then enable it 3. Check the update key

- **Update chip key:** The chip key can be updated only for UART communication interfaces. This configuration indicates that the key of the corresponding partition of the target chip is updated before the download is performed using the new key. After checking, a dialog box will pop up as shown in the figure:



**Update chip key**

USER1

Old Key:

New Key:

☒ update key ☒ First update

USER2

Old Key:

New Key:

☒ update key ☒ First update

USER3

Old Key:

New Key:

☒ update key ☒ First update

Device key:

OK Cancel ☐ Show key

Figure 8-4 Update chip key

- ✧ **Partition:** indicates the partition user1/2/3
  - ✧ **Update key:** Check to indicate whether to update the new chip key to the target chip, and use the new key to download when downloading, unchecked means to download only with the new key when downloading, but the new key will not be used. configured into the target chip.
  - ✧ **First update:** It means that the chip has not been updated after leaving the factory. The user updates the chip key for the first time. After checking this, the user does not need to enter the old chip key, and only checks the chip with the unmodified key at the factory.
  - ✧ **Old chip key:** If it is the first time to update the key, it defaults to one of the 32 sets of passwords from the factory, which does not need to be filled in by the user. Otherwise, the user's last updated key value
  - ✧ **New Chip Key:** Indicates the current key to be updated.
  - ✧ **Device key:** indicates the key of the current downloader, the default is the SN serial number of the downloader
- Note:** If the target chip needs to create a new project for program download after it has updated the key of the excessive zone, cancel "Initial update", fill in the current key value of the target chip in both "old chip key" and "new chip key", and fill in "device key". Click the ok button.

**There are several operations to update the target chip:**

update key		
	Key not updated after factory (default key)	The key has been updated since the factory
<b>Requires current chip key for download (encrypted or authenticated)</b>	No action required	1. Fill in the old key (the current key of the chip) 2. Fill in the new key, which is the same as the old key 3. Fill in the downloader device key
<b>You need to modify the current key and then</b>	1. Check Update Key 2. Check the first update 3. Fill in the new chip key	1. Check Update Key 2. Fill in the old key (the current key of the chip)

<b>use the new key to download (encryption or authentication)</b>	4. Fill in the downloader device key	3. Fill in the new key 4. Fill in the downloader device key
---	--------------------------------------	--

**Configuration option byte:** This operation indicates the configuration option byte (including read protection level, FLASH page write protection, dataA0/1 configuration, and USER configuration). For details about option bytes, refer to the corresponding chip user manual based on the chip model. The byte options for different series of chips may vary, please refer to the user manual for details, Taking the N32H473 and N32H78X\_H76X series as an example, as shown in the figure:

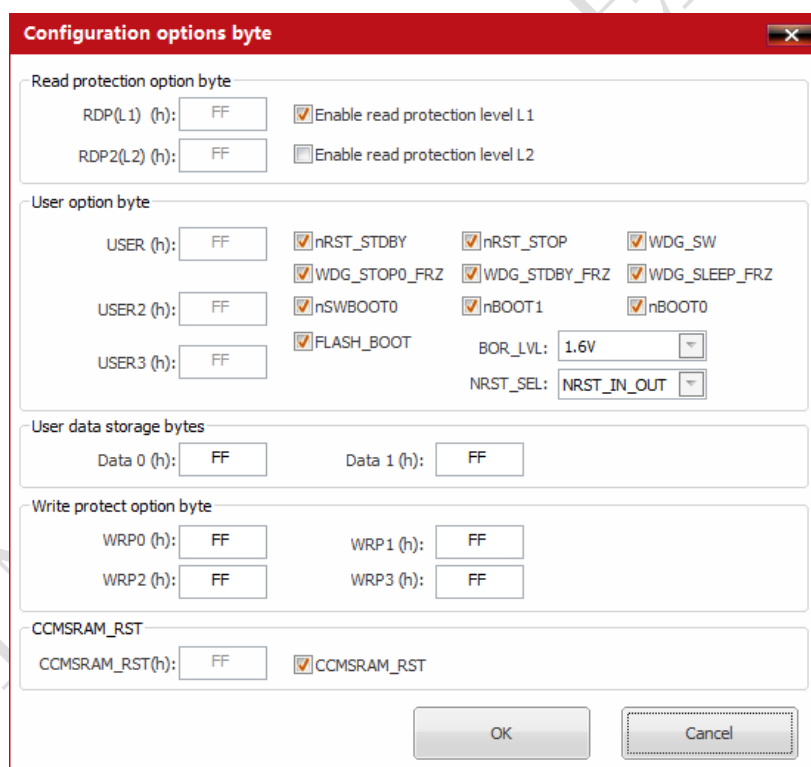
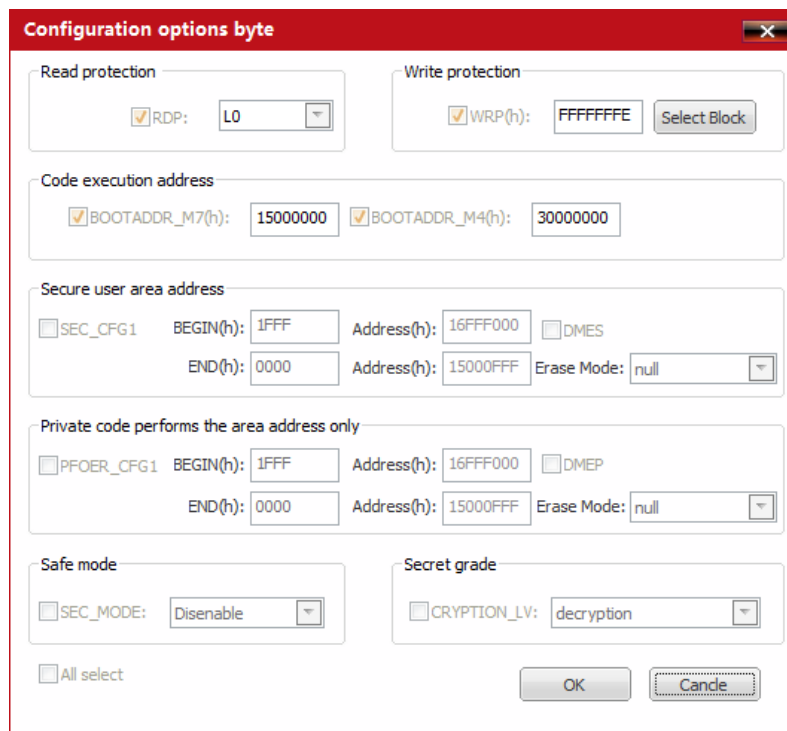


Figure 8-5 Configuration option bytes

After selecting the N32H78X\_H76X series and clicking on the configuration option byte, a dialog box will pop up as shown in the figure:



The dialog box titled "Configuration options byte" contains several sections for configuring device options:

- Read protection:** Includes a checkbox for RDP (checked) and a dropdown menu set to "L0".
- Write protection:** Includes a checkbox for WRP (checked), a text field for WRP(h) set to "FFFFFFFE", and a "Select Block" button.
- Code execution address:** Includes checkboxes for BOOTADDR\_M7(h) (checked) and BOOTADDR\_M4(h) (checked), with text fields for their values: "15000000" and "30000000" respectively.
- Secure user area address:** Includes a checkbox for SEC\_CFG1 (unchecked), text fields for BEGIN(h) (1FFF) and END(h) (0000), and a section for Address(h) (16FFF000) and Address(h) (15000FFF) with an Erase Mode dropdown set to "null".
- Private code performs the area address only:** Includes a checkbox for PFOER\_CFG1 (unchecked), text fields for BEGIN(h) (1FFF) and END(h) (0000), and a section for Address(h) (16FFF000) and Address(h) (15000FFF) with an Erase Mode dropdown set to "null".
- Safe mode:** Includes a checkbox for SEC\_MODE (unchecked) and a dropdown menu set to "Disenable".
- Secret grade:** Includes a checkbox for CRYPTON\_LV (unchecked) and a dropdown menu set to "decryption".
- All select:** A checkbox at the bottom left.
- Buttons:** "OK" and "Cancel" buttons at the bottom right.

Figure 8-6 .Configuration option bytes

Note: The N32H78X\_H76X series 1A version currently does not support the configuration of SEC\_CFG1, PFOER\_CFG1, SEC-PODE, and CRYPTON-LV.

**Read protection option byte:** User code in Flash can be set to read protection to prevent unauthorized reading. Read protection mainly protects the access operation of the main memory area and option byte block after the chip is sealed. Read protection is set by RDP bytes in the configuration option byte block. Three different read protection levels can be configured, as listed below:

Read protected state	RDP1	nRDP1	nRDP2	RDP2
L1 level	0xFF	0xFF	RDP2! = 0xCC    nRDP2! = 0x33	
Does not protect	0xA5	0x5A	RDP2! = 0xCC    nRDP2! = 0x33	
L2 level	0XX	0XX	0x33	0xCC
L1 level	None of the preceding three configurations			

Read protection configuration list

■ Level of L0:

- ◆ In the unprotected state, corresponding to (RDP1== 0xA5&NRDP1 ==0x5A) && (RDP2!=0xCC | nRDP2!= 0 x33);
- ◆ Main storage and option byte blocks can be read arbitrarily;

- ◆ You can configure the write protection properties of each Page for programming and erasure.

■ L1 levels:

- ◆ The corresponding  $\sim((RDP1 == 0xA5 \& nRDP1 == 0x5A) \&\& (RDP2 != 0xCC \mid nRDP2 != 0x33) \mid (RDP2 == 0 \& nRDP2 \neq 0))$ ;
- ◆ Read operations to the main storage area are allowed only from user code, that is, if the program is launched from the main flash memory in a non-debugging manner;
- ◆ Pages 0~1 are automatically write protected;
- ◆ Other pages can be programmed with code executed in the main flash memory (for things like IAP or data storage);
- ◆ All pages are not allowed to be written or erased (except for whole wipe) in debug mode or after booting from internal SRAM;
- ◆ All functions of loading and executing code into the built-in SRAM via JTAG/SWD are still valid, and can also be enabled from the built-in SRAM via JTAG/SWD. This function can be used to remove read protection.
- ◆ When the read protected option byte is overwritten to the unprotected L0 level, the entire main storage area is automatically erased as follows :(erasing option byte blocks does not result in an automatic whole erase operation, as the result of erasing is 0xFF, which is equivalent to still being protected at L1 level)
  - Write the correct sequence of keys to the OPTKEY unlock option byte area;
  - The bus initiates the command to erase the entire option byte area (Page erase);
  - Bus write read protection option byte 0xA5;
  - Internal automatic erasure of all main storage areas;
  - Internally write 0xA5 to read protection option bytes;

- System reset (such as software reset, etc.), option byte blocks (including the new RDP value 0xA5) will be reloaded into the system, and read protection will be removed;
- ◆ The following operations on the flash memory are prohibited:
  - Access to primary flash memory by executing code from the built-in SRAM, including using DMA;
  - Access the main flash memory through JTAG, SWV (serial line viewer), SWD (serial line debugging) and boundary scan;
- ◆ L2: this level is the same as L1 except that the debugging mode is disabled and the protection level cannot be changed (irreversible). The L2 level is achieved by configuring another option byte RDP2, regardless of the value of RDP1, as long as (RDP2==0xCC & nRDP2==0x33) the LEVEL is L2.

➤ **User option bytes:**

**USER:**

- ✧ The USER [and] : Reserved
- ✧ USER[2] : nRST\_STDBY configuration option
  - 0: A reset occurs when the standby mode is entered
  - 1: The standby mode does not reset
- ✧ USER[1] : nRST\_STOP configuration option
  - 0: reset occurs when entering STOP mode
  - 1: No reset occurs when entering the STOP mode
- ✧ USER[0] : WDG\_SW configuration option
  - 1: hardware watchdog
  - 0: software watchdog

**USER2:**

- ✧ USER2 [7] : Reserved
- ✧ USER2[6:4] : BOR\_LEV[3:0], default is 0

- ✧ USER2 [3] : Reserved
- ✧ USER2[2] : nSWBOOT0 configuration option, default is 1
- ✧ USER2[1] : nBOOT1 configuration option, default is 1
- ✧ USER2[0] : nBOOT0 configuration option, default is 1

#### Write protection option bytes:

- ✧ WRP0: write protection for pages 0 to 15
- ✧ WRP1: write protection for pages 16 to 31
- ✧ WRP2: write protection for pages 32 to 47
- ✧ WRP3: write protection for pages 48 to 255

- **Write sequence number:** indicates the write sequence number, including the write address, start value, and step value. Formula for calculating the serial number: 4 bytes Serial number value = (start value + step value x number of successful downloads);

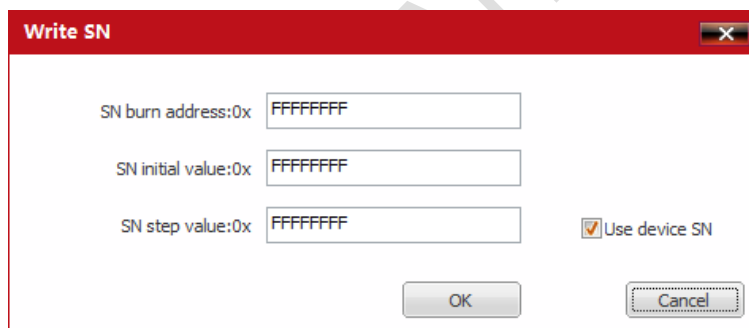


Figure 8-7 Writing the serial number

**Note:** Serial numbers start with "serial number (SN) burn address", take up 32 bytes of space, must be all 0xFF (no value).

- a) If use downloader serial number is not selected, the sequence number will be written to the first 4 bytes of the 32 byte space and the last 28 bytes will be written to 0xFF.

32 bytes space	
4 bytes serial number value	28 bytes 0 XFF

- b) Check if the "use downloader serial number", is in the download program, put downloader serial number sequence number value after each equipment serial

number (the only), serial number of 20 bytes (16 bytes downloaded serial number + serial number 4 bytes), and to write serial number 20 bytes into 32 bytes before 20 bytes of the space, the remaining 12 bytes of 0 XFF.

32 bytes space		
16-byte download serial number	4 bytes serial number value	All 12 bytes are 0xFF

- **New project:** Create a new project and initialize the parameters of the project
- **Delete item:** Delete an existing item in the downloader
- **Active project:** sets the current project to the one currently used by the downloader
- **Open a project file:** Opens an existing project file (\*.nspf). It can only be opened for viewing but cannot be modified
- **Save the project file:** Save the configured project to a local computer in a \*. NSPF file
- **Save project to Downloader:** Save the currently configured or opened project to downloader
- **Start download to chip:** Downloads the current item from the downloader to the chip

### 8.1.3 Making an encrypted file

Making encrypted files encrypts downloaded files so that the downloaded files can be transmitted and saved in encryption.

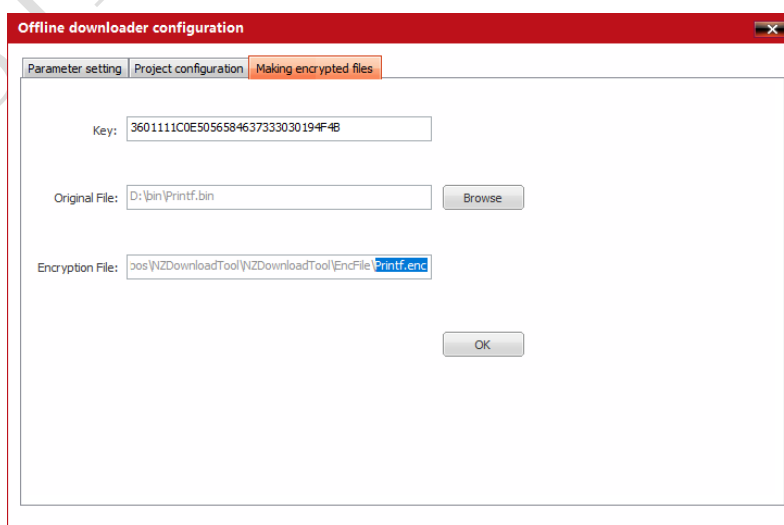


Figure 8-7 Making an encrypted file



- **Key:** serial number (SN), the key used to encrypt the original file. The length is 16 bytes.
- **Original file:** The original file to be encrypted. The file can be in \*. Hex or \*. Bin format
- **Encrypted file:** an encrypted file in \*. Enc format

## 8.2 SWD mode download configuration example

SWD download is a common download interface. Users can configure the download interface of the download device as a four-line SWD interface through the upper computer. SWD mode download is suitable for hand-held download device for small batch program burning, also can be paired with machine for mass production burning. **Note: offline download will release the original read-write protection in the chip by default.**

### 8.2.1 Download the project configuration offline

- 1、 Click "Offline Downloader Configuration", the offline project configuration dialog box pops up.

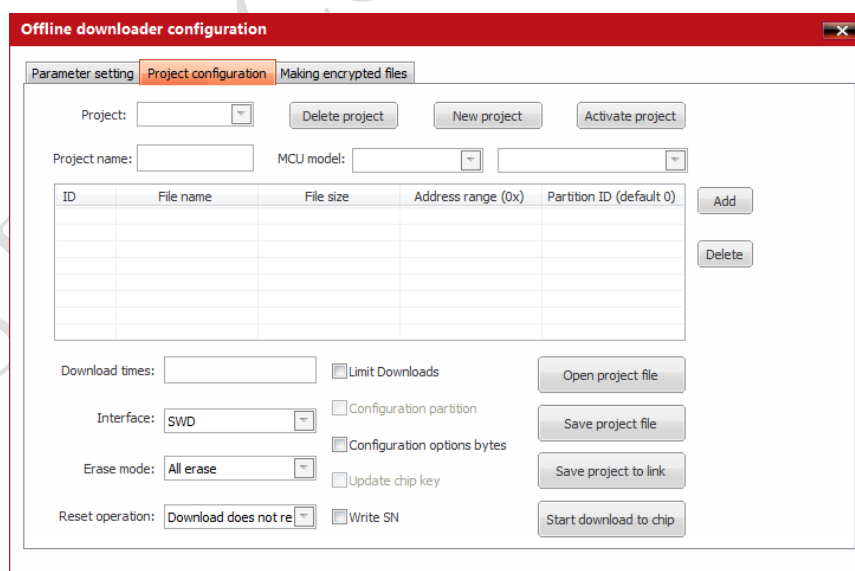


Figure 8-9 Click offline Downloader configuration

- 2、 Click New Project.
- 3、 Fill in the project name, the project name cannot exceed 32 bytes

- 4、 Select a chip model from the drop-down list box,different series of chips have different configurable parameters.
- 5、 Download times. If you need to limit the download times, check the limit and fill in the download times. If not checked, there will be no limit.
- 6、 The communication interface can choose between SWD or USART, while the SWD interface cannot be configured with partitioning or updating chip keys.Erasing mode select full - slice erasing.
- 7、 The erase mode can choose to erase the entire chip or erase by file size.
- 8、 The reset operation can choose to download without resetting or reset after downloading.
- 9、 Configure option bytes. If checked, configure option bytes as needed. If unchecked, do not configure.
- 10、 Write the serial number, check it to modify the serial number as needed, and do not modify it if not checked.
- 11、 Click Add and select the file you want to download.
- 12、 In the dialog box that pops up, fill in the address 0x08000000 for downloading files to the target chip (0x08000000 address is the start flash address of the chip) and click "OK".

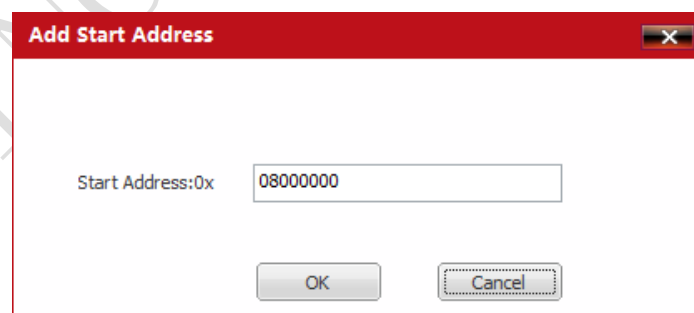


Figure 8-10 Adding a file

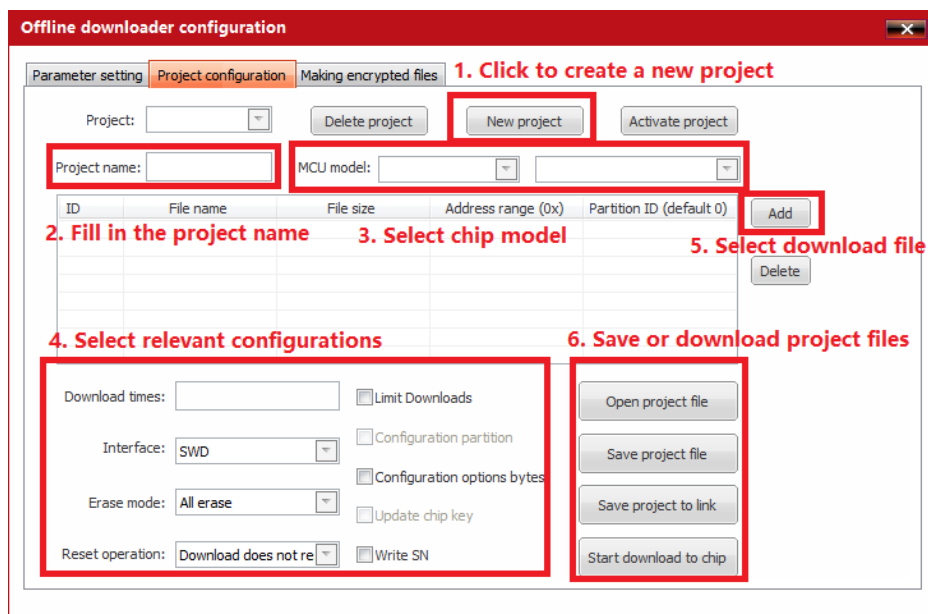


Figure 8-11 Configuring the offline downloader project

- 13、 Click "Save project file", the project setting dialog box pops up, uncheck the two selection boxes, and click "OK".

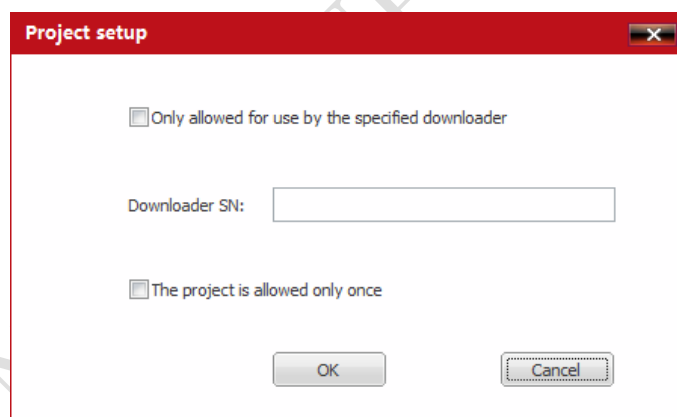


Figure 8-12 Project Settings dialog box

- 14、 In the dialog box that is displayed, select Yes.

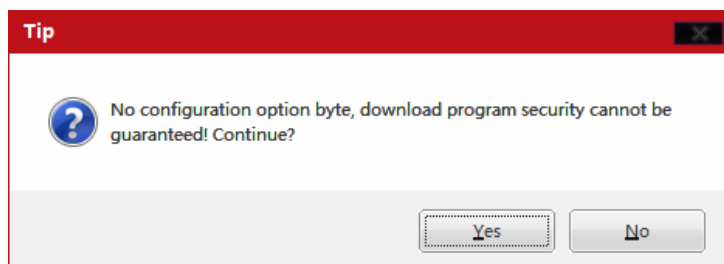


Figure 8-13 Click "Yes"

- 15、 Select a file storage path, enter a file name, and click Save.

- 16、 After successful saving, if an offline downloader is connected, you can directly click the "Save Project to Downloader" button or send the project file to a third party for download.

**Note: For N32H78X\_H76X series chips:**

- a) If the JTAG mode of the chip is disabled, SWD download is not supported
- b) If the chip enables safe mode, SWD download is not supported
- c) If the chip is configured with PFOER area, the download address overlaps with the PFOER area address and cannot be downloaded

## 8.2.2 Save the project to an offline downloader

- 1、 Select "NS Link Pro" for the interface, click "Connect Device", and connect the upper computer to the downloader. If the connection is successful, the device information will be printed and a project configuration dialog box will pop up, as shown in the figure:

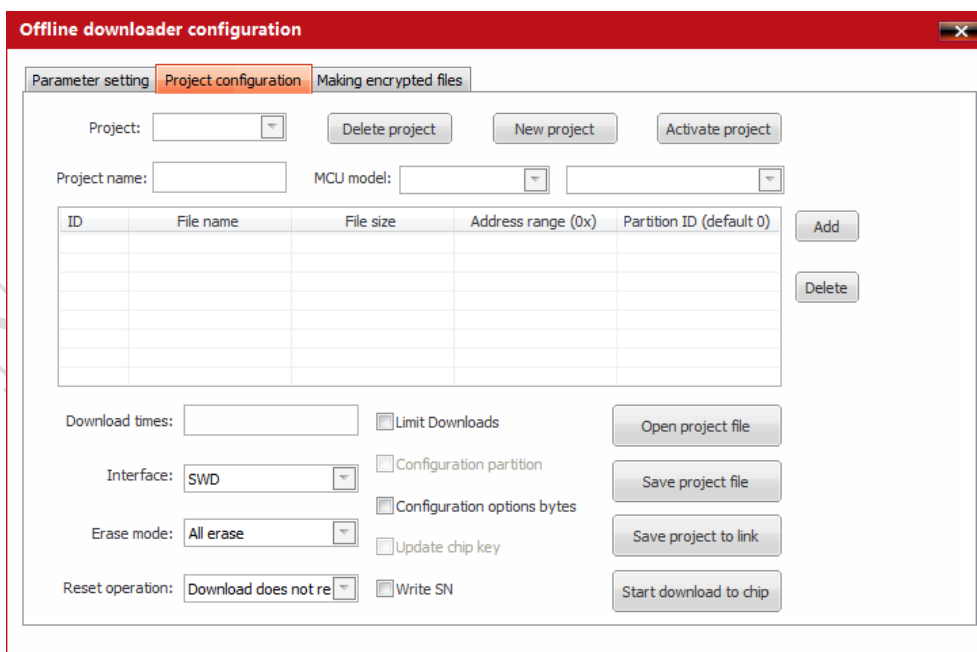


Figure 8-14Project Configuration

- 2、 Click "Open project File", select the project file in 5.5.1 Save to local, and click "Open".

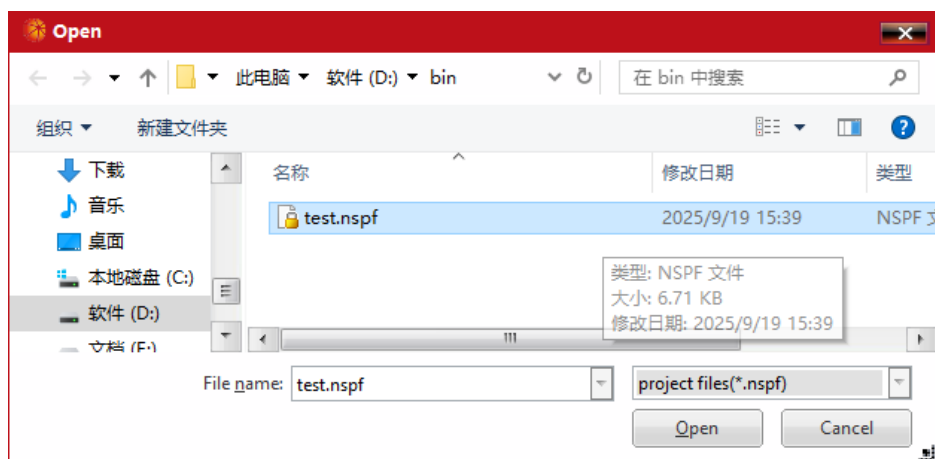


Figure 8-15 Selecting an existing project file

3、Click OK.

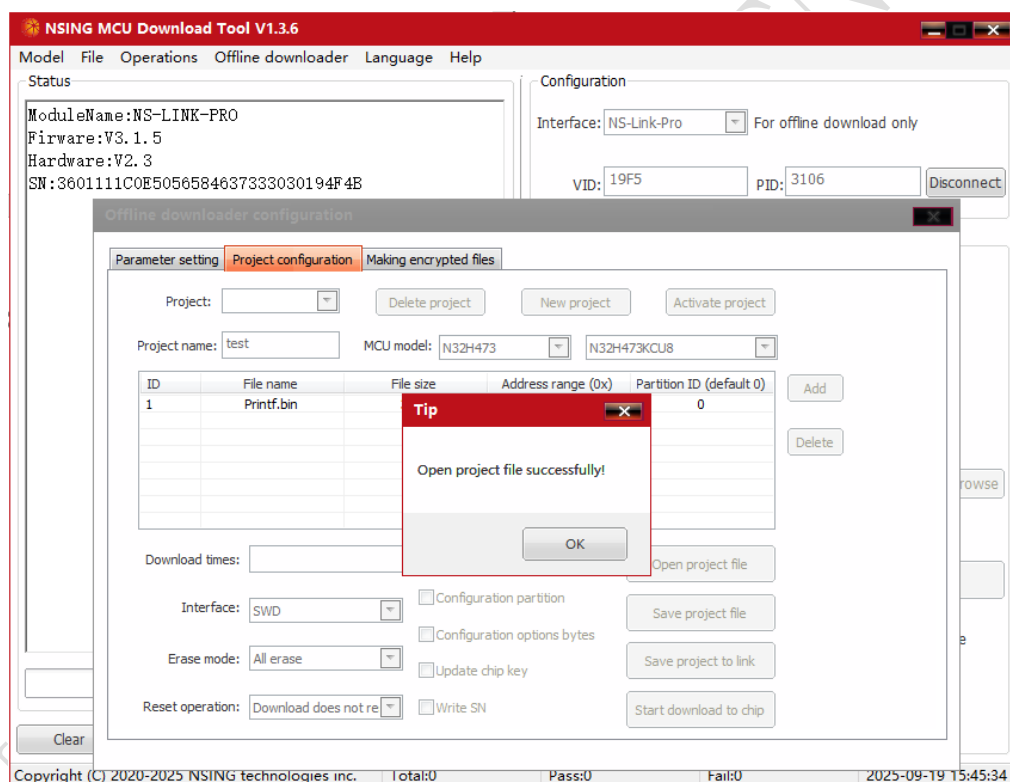


Figure 8-16 Opening the project

- 4、Click "Save project to Downloader".
- 5、Wait for the project transfer to complete.
- 6、When the project is transferred, click OK.

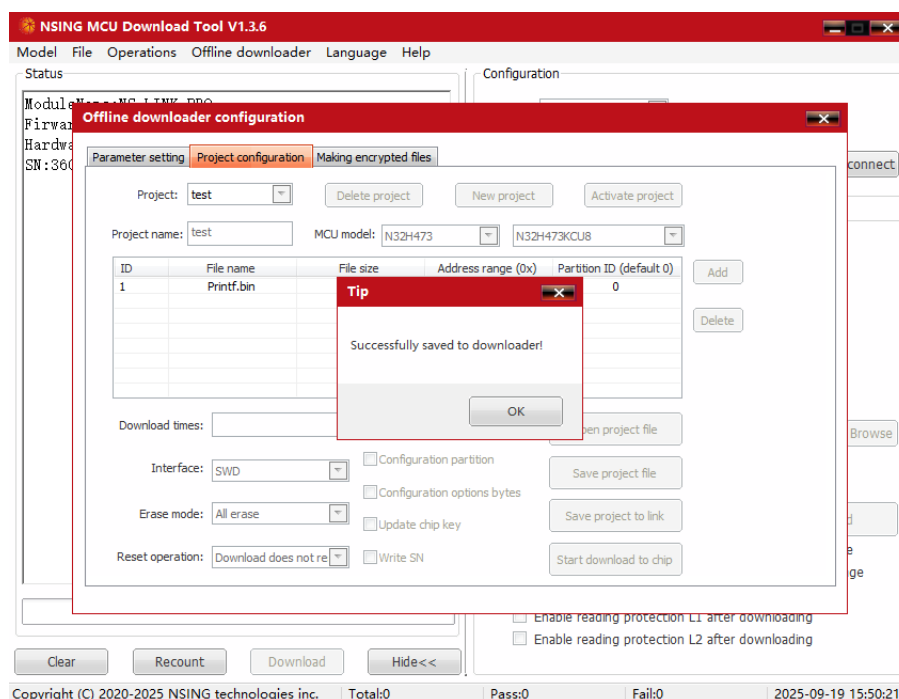


Figure 8-17 Project transfer completed

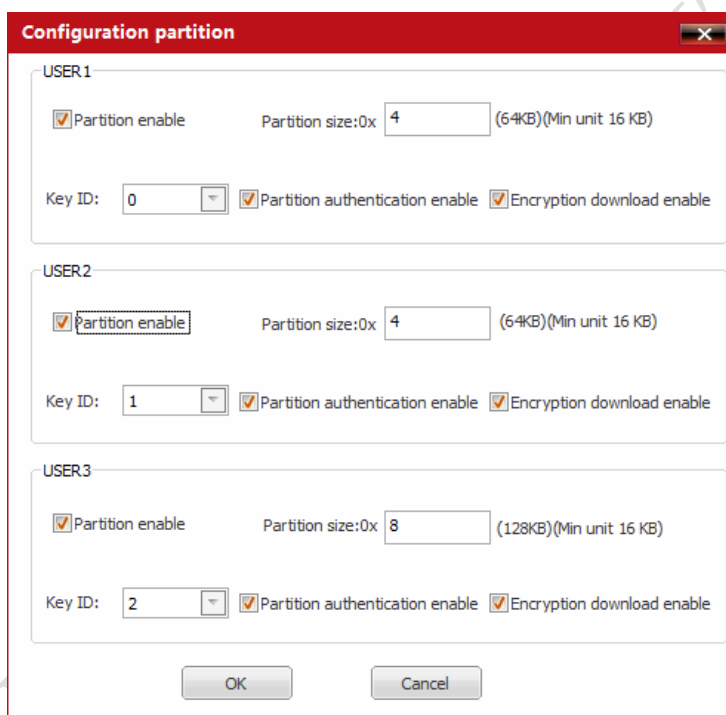
## 8.3 UART(serial port) mode download configuration example

Serial mode download is through the security BOOT program solidification in the MCU for code download, can support a variety of MCU security partition, security encryption and transmission, security authentication and other unique security features and download mode, so that the data between the download device and the chip can be safe and efficient transmission.

### 8.3.1 Offline Project Configuration

- 1、Click on 'New Project'.
- 2、Fill in the project name, which cannot exceed 32 bytes
- 3、Select the chip model from the dropdown menu.
- 4、Download times. If you need to limit the download times, check the limit and fill in the download times. If not checked, there will be no limit.
- 5、Select UART as the communication interface
- 6、The reset operation can choose to download without resetting or reset after downloading.

- 7、 The erase mode can choose to erase the entire chip or erase by file size
- 8、 Partition configuration is limited to the series of chips that support partitioning. If checked, partition configuration will be carried out as needed. If unchecked, partition configuration can be set to partition size. The key ID can be selected for encryption download enable and partition authentication enable, and the key ID. Note: Due to the irreversibility of partition configuration, caution should be exercised during configuration.



**Configuration partition**

**USER 1**

☒ Partition enable      Partition size:0x  (64KB)(Min unit 16 KB)

Key ID:   ☒ Partition authentication enable ☒ Encryption download enable

**USER 2**

☒ Partition enable      Partition size:0x  (64KB)(Min unit 16 KB)

Key ID:   ☒ Partition authentication enable ☒ Encryption download enable

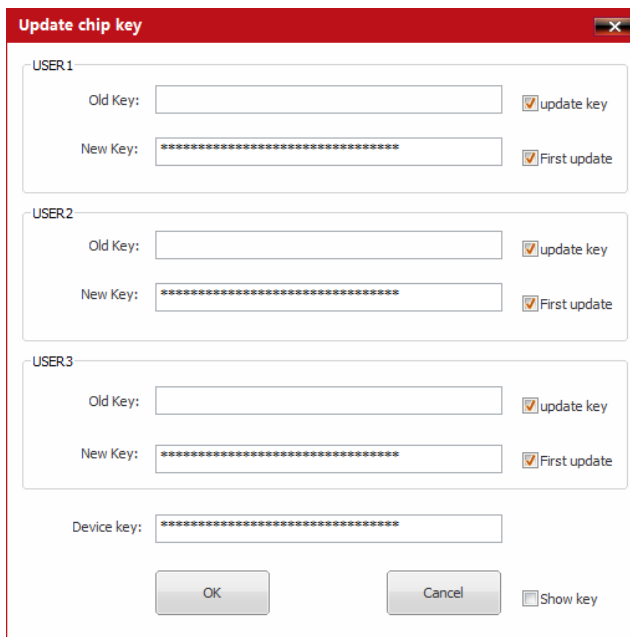
**USER 3**

☒ Partition enable      Partition size:0x  (128KB)(Min unit 16 KB)

Key ID:   ☒ Partition authentication enable ☒ Encryption download enable

Figure 8-18 Partition Configuration

- 9、 Update chip key, limited to the series of chips that support partitioning. Check to update chip key, uncheck not to update. Check to update key to update the current partition key, otherwise not to update. Check not to enter old key for initial update, otherwise old key is required.



**Update chip key**

USER1  
 Old Key:  ☒ update key  
 New Key:  ☒ First update

USER2  
 Old Key:  ☒ update key  
 New Key:  ☒ First update

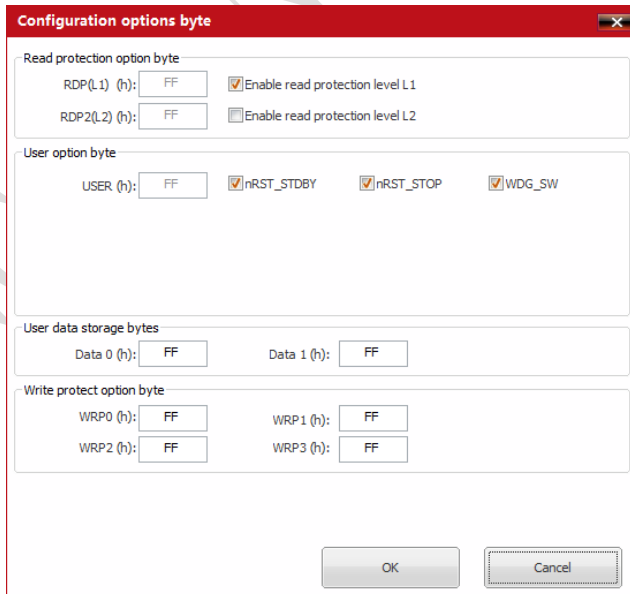
USER3  
 Old Key:  ☒ update key  
 New Key:  ☒ First update

Device key:

OK Cancel ☐ Show key

Figure 8-19 Update chip key

- 10、 Configure option bytes. If checked, the option bytes will be configured according to the needs. If unchecked, the display interface will vary for different series of chips, as shown in the figure:



**Configuration options byte**

Read protection option byte  
 RDP(L1) (h):  FF ☒ Enable read protection level L1  
 RDP2(L2) (h):  FF ☐ Enable read protection level L2

User option byte  
 USER (h):  FF ☒ nRST\_STDBY ☒ nRST\_STOP ☒ WDG\_SW

User data storage bytes  
 Data 0 (h):  FF Data 1 (h):  FF

Write protect option byte  
 WRP0 (h):  FF WRP1 (h):  FF  
 WRP2 (h):  FF WRP3 (h):  FF

OK Cancel

Figure 8-20 Configure option bytes

- 11、 Write the serial number, check it to modify the serial number as needed, uncheck not to modify



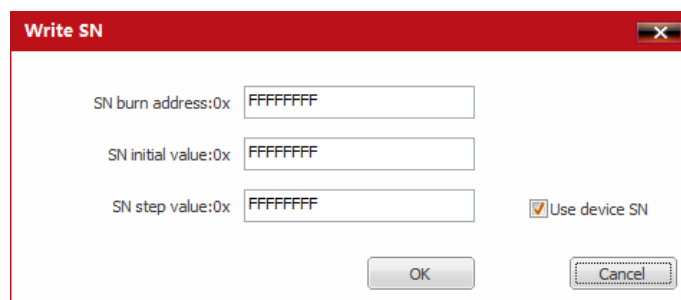


Figure 8-21 Write the serial number

- 12、 Select the file you want to download, click "Open", and in the pop-up dialog box for adding a starting address, select the downloaded partition and fill in the starting address, such as 0x08000000 (the starting address of partition 1 is the starting address of the chip FLASH). The maximum number of files that can be selected is 8.

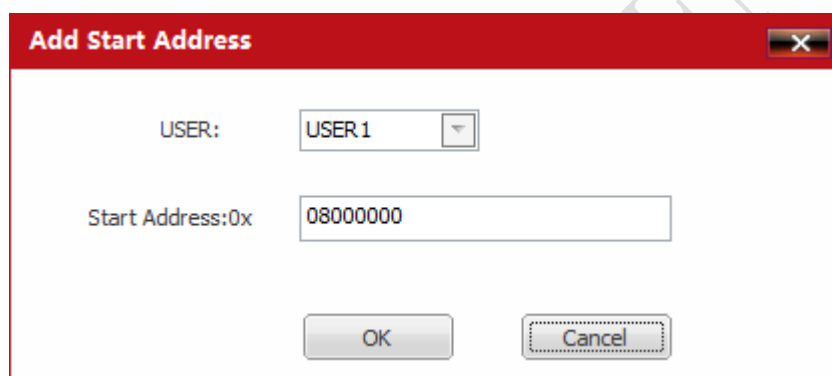


Figure 8-22 Select partition, fill in download start

- 13、 Click 'Add' and select the download file

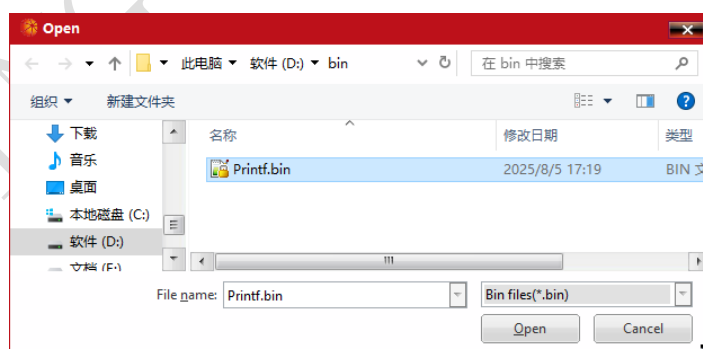


Figure 8-23 Select the files that need to be downloaded

- 14、 Click 'Save Project File' to save the project file locally. Or click "Save Project to Downloader",

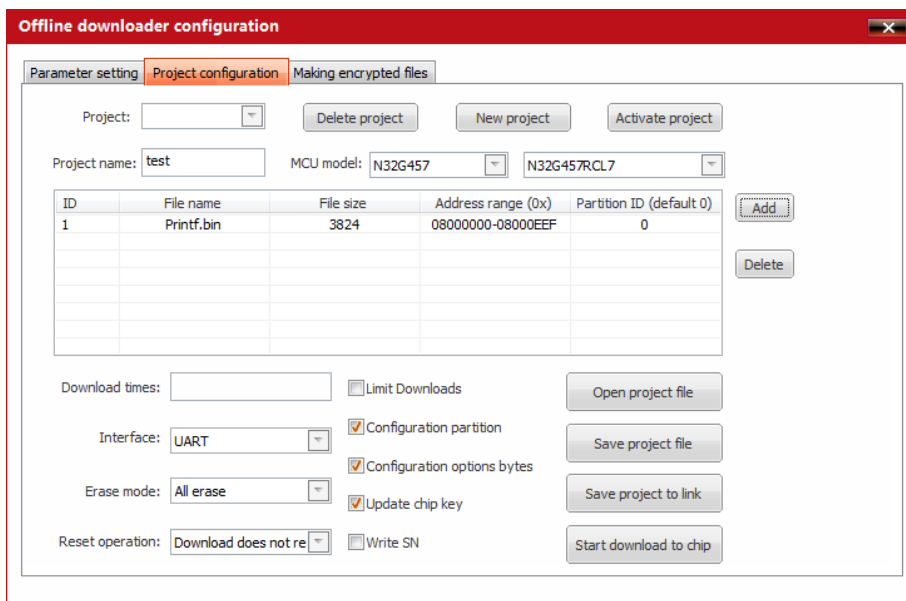


Figure 8-24 Save project file or save project to downloader

**Note:** When downloading multiple files, files smaller than one page must occupy one or two separate pages (in the case of cross page), and the download start and end addresses of other files must not be on the same page (for files smaller than one page), otherwise the download will fail.

### 8.3.2 Save Project to Offline Downloader

Refer to 8.2.2

## 8.4 Offline downloader external interface

The external interfaces of offline downloader are defined as follows (note that the interface of offline downloader is not a standard JTAG interface, and it is forbidden to use the standard JTAG cable for access) :

GND	IO3	NRST	BT	IO2	SWCLK	SWDIO	IO1	VT	GND
5V	GND	RX_SDA	TX_SCL	ERROR	PASS	BUSY	START	GND	3V3

Figure 8-25 Interface definition

**3V3:** 3.3V voltage output

**5V:** 5V output voltage

**VT:** The output voltage can be configured through the upper computer. When no VT output is configured, the external power supply can be connected through VT. When the upper computer configures the holding time of output voltage after downloading, the output will be kept after downloading, and the VT power output will be shut down after the setting time. Reset control can be used to check that the downloaded code is running correctly while the output is held.

**SWDIO:** SWD data download interface

**SWCLK:** SWD clock download interface

**BT:** BOOT0 control pin for serial port download

**NRST:** reset control pin, external download chip reset pin

**START:** machine download control signal

**BUSY:** The machine controls the BUSY signal

**PASS:** indicates the successful control signal of the machine

**ERROR:** indicates that the machine control fails

**TX\_SCL:** indicates the TX output of the serial port

**RX\_SDA:** serial port RX input

**IO1, IO2, and IO3:** reserved

**Dip switch:** Turn OFF (towards USB interface), single download mode (default)

**Dial to ON** (towards the download interface), continuous download mode (not recommended)

**Button S1:**

Main interface: single download start button.

Other interface: Select operation.

**Button S2:**

Press to confirm or enter the next-level menu.

Long press: Return or exit.

## 8.5 Offline downloader sound and light status information

	LED3			LED2			LED1			buzzer
	red	yellow	green	red	yellow	green	red	yellow	green	
power on	off	off	One flash	off	off	One flash	off	off	One flash	A short sound
spare	off	Change according to download mode	off	off	According to download mode		off	off	on	quiet
Offline download	off	Change according to download mode	off	off	According to download mode		off	off	Quick flicker	quiet
Download successful	off	Change according to download mode	off	off	According to download mode		off	off	on	A short sound
Download failed	off	Change according to download mode	off	off	According to download mode		Quick flicker	off	off	Emergency quick sound for 3s
The number of downloads is 0	on	off	off	on	off		Quick flicker	off	off	Emergency quick sound for 3s
The device key does not match the file encryption key	off	off	off	on	off	off	Quick flicker	off	off	Emergency quick sound for 3s
Continuous download mode	off	Change according to download mode	off	off	on		Changes according to the running state			
Single download mode	off	Change according to download mode	off	off	off	off				
SWD download mode	off	on	off	off	According to download mode					
Serial Port Download mode	off	off	off	off	According to download mode					
Firmware Update Mode	off	off	off	off	off		off	flashing	off	quiet

Figure 8-26 Sound and light information

## 8.6 The machine controls the timing

1. All levels are valid at high levels, and pulse width of PASS and ERROR effective levels is 0, that is, signal output level.

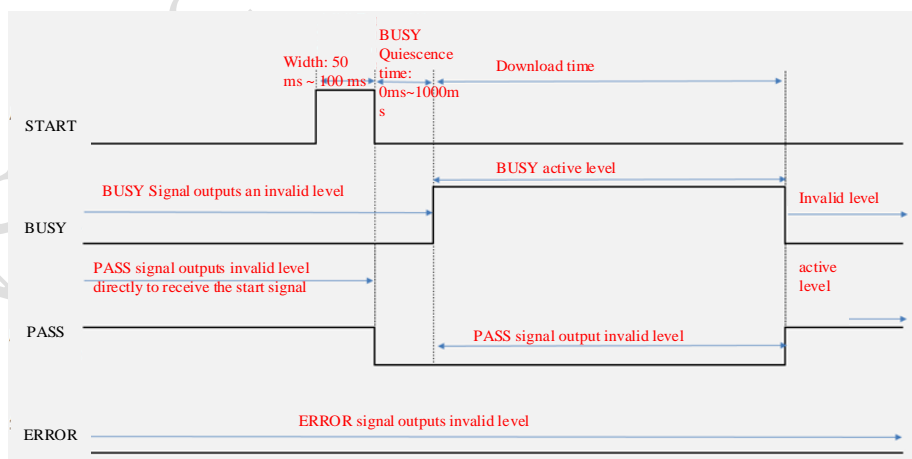


Figure 8-64 Sequence diagram of successful download

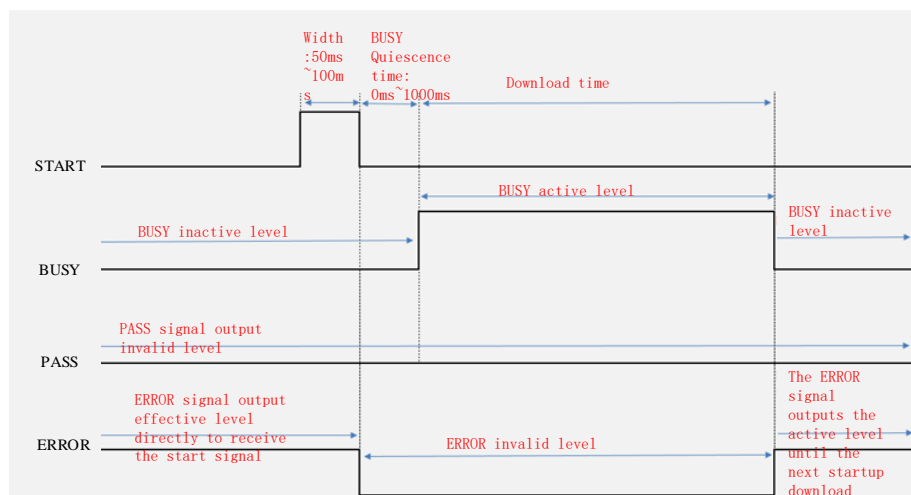


Figure 8-27 Download failure sequence diagram

2. The high level of START and BUSY is valid, while the low level of PASS and ERROR is valid. The pulse width of the effective level is not 0, that is, the signal output pulse.

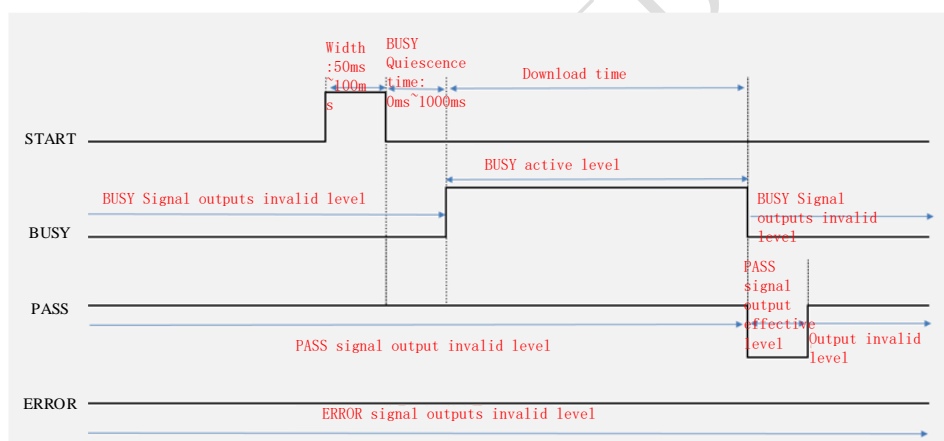


Figure 8-66 Download succeeded

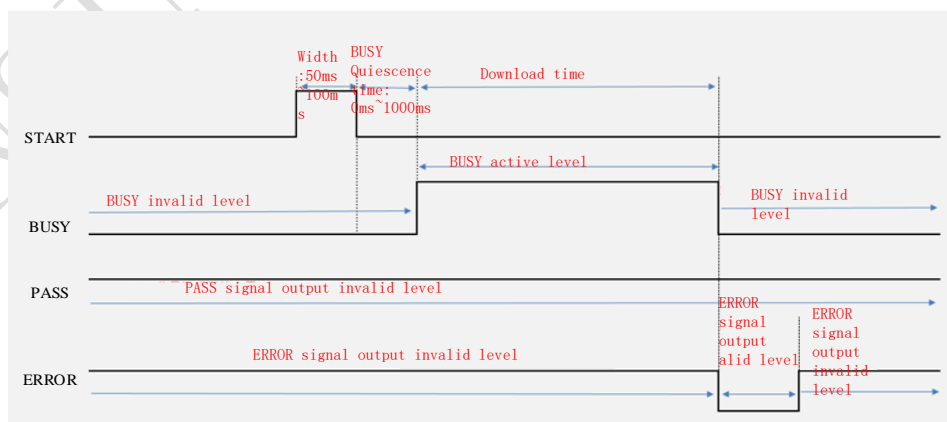


Figure 8-28 Download failed

## 8.7 Multipath download control

Ns-link-pro offline downloader is a single channel downloader, each downloader has a separate machine control signal. When the user needs to use multi-channel download multiple chips, only need to use multiple devices to load the download file, by the machine separately connected to each download, and control, can be composed of multi-channel download. The connection diagram between the machine and the downloader is as follows:

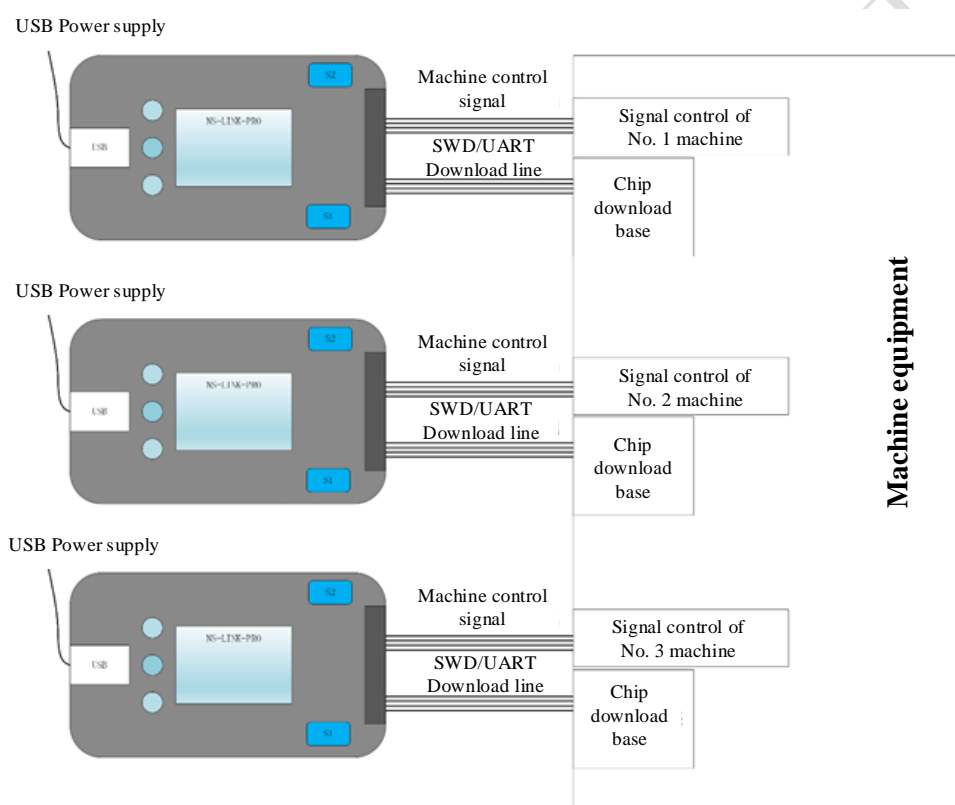


Figure 8-29 Schematic diagram of multi-way download connection

## **9 Common Errors and Solutions**

### **9.1 Bad download of onboard NS\_LINK serial port**

Phenomenon: The download speed is very slow, or the progress bar is stuck in the middle of the download, and the baud rate of the serial port is increased, and the speed increase is not obvious.

Reason: The NS\_LINK serial port of the board is a virtual serial port implemented by software. On the NS\_LINK main control chip, the data is parsed through the USB interface and then transferred to the serial port and sent to the MCU. This process is much more complicated than the independent serial port, and the data must also be considered. Packet loss problem, so it takes a long time.

Solution: Use an independent USB-to-serial port. Generally, it is recommended to use a serial port tool whose main control is CH340 or MAX232.

### **9.2 Bad download of independent serial port**

#### **9.2.1 The serial port cannot be connected**

Phenomenon 1: The serial port cannot be connected to the chip, no matter which baud rate is selected, the connection fails;

Reason: The chip may not enter the BOOT0 mode, and the TX of the serial port tool may reverse current to the chip, resulting in failure to enter the BOOT state;

Solution: The power-on sequence of VDD, BOOT0 and serial port is: 1. Pull up BOOT0; 2. Supply power to the VDD of the chip; 3. Access the serial port tool;

Phenomenon 2: Only one baud rate can be connected to the chip, other baud rates fail to connect

Reason: The chip may not be the latest version, and the BOOT sub-version is a chip before V2.2, which does not support automatic baud rate identification;

Solution: use the current baud rate to download, or replace the chip with a new version;

### **9.2.2 When the chip is programmed for the first time, it indicates that it is in the state of level protection L1**

Reason: Due to factors such as unstable power-on, L1 level protection is automatically turned on inside the chip;

Solution: After connecting, select "Release L1 read protection level L1" in common operations to release the read protection level L1 state;

### **9.2.3 Download bin file and hex file, the software behavior of the two is inconsistent**

The object files compiled in the development environment generally include three files: Bin, Hex and Axf.

Bin file: the most direct code image;

Hex file: In addition to the code itself, it also contains the address information of the program;

Axf file: The file generated by default for compilation, not only contains code data, but also contains debugging information. This file is used for debug debugging in MDK.

Abnormal phenomenon: The bin file and hex file compiled by the same project are burned to the same board, and the software behavior is different. After burning the hex file, the program does not run or runs away, but the program that burns the bin file executes normally.

Reason: When the NSING MCU Download Tool tool downloads the hex file, it will first decode the hex file, convert it into a bin file, and then burn it to the chip. During the conversion process, redundant data may appear in some areas, resulting in program exceptions.

Solution: Update NSING MCU Download Tool and use V1.2.5 or above; or use third-party tools such as JFlash to download firmware.

## **9.3 USB does not recognize the device**

Reason 1: The DFU device driver is not installed on the user's computer;

Solution: In the driver\USB DFU folder in the tool directory, choose to install the USB driver corresponding to the system, and then the device can be connected normally;



Reason 2: If this happens on the development board, it may be caused by the conflict between the serial port of NS\_LINK and the USB command. After pulling up BOOT0 to return to the BOOT state, the serial port connection will be used first by default, so the serial port of NS\_LINK will be connected first, resulting in an abnormal USB connection.

Solution: Before pulling up BOOT0, first unplug the serial jumper cap of NS\_LINK on the development board, and then enter the BOOT state.

## **9.4 Bad SWD download**

### **9.4.1 Unable to connect chip**

Reason 1: The driver is not installed;

Solution:

1. If using an offline downloader, check if the dip switch is OFF;
2. If an offline downloader is used, the VT pin cannot be used for power supply (VT is only used for offline downloads);
3. Install the corresponding system driver in the driver \ CMSIS DAP CDC path in the tool directory. The offline downloader is poorly programmed

### **9.4.2 NS\_LINK cannot connect**

Reason 1: The driver is not installed;

Solution: Install the driver for the corresponding system in the driver\CMSIS DAP CDC path in the tool directory.

### **9.4.3 Offline download project cannot be saved**

Phenomenon: After configuring the download project, saving to the downloader fails, prompting "Project name already exists"

Reason 1: There is already a project with the same name in the downloader;

Solution: 1. Delete the items that exist in the downloader;

2. Change the name of the currently downloaded project

## 10 Version history

Version	Date	Modification point
V1.1.1	2019-12-3	first version, support N32G(WB)45x_FR series chips
V1.1.2	2020-2-20	<ol style="list-style-type: none"> <li>1. Increase the display of chip model</li> <li>2. Modify the problem of CRC check error when enabling encrypted download and checking the downloaded file as cipher text</li> <li>3. When the encryption download is disabled, it is not allowed to check the download file as ciphertext</li> <li>4. Increase and modify the baud rate</li> </ol>
V1.1.3	2020-4-16	<ol style="list-style-type: none"> <li>1. Optimize the process of connecting devices</li> <li>2. Added support for USB (DFU) interface</li> </ol>
V1.1.4	2020-8-10	<ol style="list-style-type: none"> <li>1. Modify the erasure range display error problem</li> <li>2. Optimize the interface</li> </ol>
V1.1.5	2020-9-20	<ol style="list-style-type: none"> <li>1. Put the configuration partition into the advanced configuration</li> <li>2. Optimize the interface</li> </ol>
V1.1.6	2020-9-28	<ol style="list-style-type: none"> <li>1. Optimize the display of chip information</li> <li>2. Optimize the configuration partition</li> <li>3. Modify the size limit of the serial port number</li> </ol>
V1.1.7	2020-10-28	<ol style="list-style-type: none"> <li>1. Added support for N32G432, N32G435, N32L43X, N32L40X, N32G030, N32G032 series chips</li> </ol>
V1.1.8	2020-12-24	<ol style="list-style-type: none"> <li>1. Added the function of making encrypted files</li> <li>2. Add multiple languages, support switching between Chinese and English</li> </ol>
V1.1.9	2020-12-30	<ol style="list-style-type: none"> <li>1. Added support for N32G031 series chips</li> </ol>
V1.1.10	2021-1-14	<ol style="list-style-type: none"> <li>1. Optimize the display of connected devices and chip information</li> <li>2. Optimize the main interface</li> <li>3. Add JLINK interface and release read protection</li> <li>4. Added support for hex file download</li> </ol>

		5. Modify the encrypted file format and add the first 4 bytes as plaintext CRC 6. Modify the print format of the diary, and print all instruction streams when it fails
V1.1.11	2021-4-25	1. Modify the problem of incorrect identification of individual chips of N32G030 and N32G032
V1.1.12	2021-5-24	1. Modify the problem of connection failure after power on and off 2. Modify the N32L40X and N32L43X chips to identify the flash size error problem
V1.2.0	2021-7-8	1. Added NS_link offline downloader related 2. Optimize the interface
V1.2.1	2021-7-27	1. Common functions added to enable read protection L1, L2 2. Optimize and update the chip key 3. Optimize the configuration partition 4. When the offline downloader saves the project, compare the partition id and the partition key id of the updated key 5. Increase the initialization of related variables when entering the offline downloader configuration and creating a new project 6. Modify the problem that the file size is 0 after the offline downloader deletes the file 7. When modifying read protection L1 L2, the first two pages cannot be downloaded, and other pages can be downloaded 8. Optimize the page number algorithm for erasing
V1.2.2	2021-10-9	1. Add write protection for common operations 2. Modify N32G030 64k read Flash size error problem 3. The chip key is encrypted and saved in the registry 4. Do not send 7F when connecting, that is, the UART interface of subsequent versions no longer supports BOOT V2.1 version 5. Add the automatic connection when the USB interface is disconnected
V1.2.3	2021-12-14	1. Added support for N32G031 series chips

		<ol style="list-style-type: none"> <li>The offline downloader adds support for N32WB031 series chips</li> <li>Add 10ms delay between erasing and downloading for N32G031, N32G030, N32G032</li> <li>Modify the problem that the color of the display content is sometimes displayed incorrectly</li> <li>Optimize the firmware update of offline downloader</li> <li>Delete the 576000 option from the baud rate selection list</li> <li>Modify the error report of the XP system open tool, and use the ini configuration file for the language pack</li> <li>Modify the problem that the win7 home version computer does not recognize the hid device correctly</li> </ol>
V1.2.4	2021-12-28	<ol style="list-style-type: none"> <li>Modify the configuration file Series CFG Table.ini and add N32G031 series chips</li> <li>Add N32G031x_NRP.FLM algorithm file</li> </ol>
V1.2.5	2022-1-5	<ol style="list-style-type: none"> <li>Added support for N32G430 series chips</li> </ol>
V1.2.6	2022-5-12	<ol style="list-style-type: none"> <li>Add SWD (CMSIS DAP) interface</li> <li>Add read protection operation before and after downloading</li> <li>Modify the multi-byte character set to unicode character set</li> <li>Increase the print download address range, check code, download time</li> <li>Main interface adjustment and other optimizations</li> <li>Added tool online upgrade and update function</li> </ol>
V1.3.0	2022-7-27	<ol style="list-style-type: none"> <li>Modify the offline downloader to open the hex file to report an error</li> <li>Under the SWD (CMSIS DAP) interface, add automatic connection when resetting and replacing devices</li> <li>When deleting an item in the offline downloader, add a progress bar</li> <li>Under the SWD (CMSIS DAP) interface, modifying the download address is not the problem of page alignment download failure</li> <li>Added online upgrade of offline downloader firmware</li> <li>Under the SWD (CMSIS DAP) interface, add the entire Flash verification after</li> </ol>

		<p>downloading</p> <p>7. Under the SWD (CMSIS DAP) interface, modifying N32G030,N32G032,N32G031 can also interpret the protection in the L1 state</p> <p>8. Added automatic pop-up prompt tool upgrade</p> <p>9. Other function optimization</p>
V1.3.1	2022-8-23	<p>1. Added support for N32A455 series chips</p> <p>2. Other function optimization</p>
V1.3.2	2023-3-6	<p>1. Added support for N32G003 series chips, offline downloader temporarily supports SWD interface download</p> <p>2. Added support for N32G401 series chips, offline downloader temporarily supports SWD interface download</p> <p>3. Offline downloader adds UART interface download supporting N32G031 series chips</p> <p>4. The baud rate is set to 115200 by default</p> <p>5. When selecting a file, record the suffix and directory of the last selected file</p> <p>6. Unlimit the minimum file size of 2k</p> <p>7. Added support for hex files with option bytes</p>
V1.3.3	2024-3-7	<p>1. Modify the FLM file(N32G003_29.5_NRD.P.FLM)</p>
V1.3.4	2024-7-22	<p>1. Modify and use instruction dynamic library</p> <p>2. Add support for N32A430 series chips</p> <p>3. Add support for N32A032 series chips</p> <p>4. Add support for N32H47X/48X series chips</p> <p>5. Add support for N32G05x series chips</p> <p>6. Modify hex files that support different address ranges</p> <p>7. Modify known bugs</p>
V1.3.5	2025-07-28	<p>1. Add support for N32H78X_H76X series chips, Online temporarily supports USART interface, offline temporarily supports SWD interface</p> <p>2. Optimize instruction dynamic library and download process</p>

V1.3.6	2025-09-22	<ol style="list-style-type: none"><li>1. Add support for N32G033 series chips, Offline downloaders are currently not supported</li><li>2. Optimize and update ,Using a new logo and name</li></ol>
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## 11 Online upgrade tool

In the online state, open the tool to judge the version, if it is not the latest version, the tool will pop up an upgrade prompt window (no network will not prompt).

If you choose to upgrade, you will be upgraded to the latest version.

If you choose not to upgrade, you will not be prompted to upgrade until the next time you open the tool; in addition, users can also select "Download tool to check for updates" in the help menu to upgrade the tool.

**Note: The online upgrade tool must be online.**

## 12 Online upgrade offline downloader firmware

In the online state, after the offline downloader is successfully connected, the firmware version of the offline downloader will be judged. If it is not the latest version, the tool will pop up an upgrade prompt window (not connected to the Internet will not prompt).

If you choose to upgrade, you will be upgraded to the latest version of the firmware.

If you choose not to upgrade, you will not be prompted to upgrade until the next time you open the tool and connect to the offline downloader successfully; in addition, the user can also select "Check the update for the offline downloader" in the help menu to upgrade the firmware of the offline downloader.

**Note: The online upgrade of the offline downloader firmware must be done in the state of the Internet.**

## 13 Notice

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